

# **16-bit MCU and DSC Programmer's Reference Manual**

High-Performance Microcontrollers (MCU) and Digital Signal Controllers (DSC)

2005-2011 Microchip Technology Inc.

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# **Section 1. Introduction**

# HIGHLIGHTS

This section of the manual contains the following major topics:

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1.2	Manual Objective	. 6
1.3	Development Support	. 6
1.4	Style and Symbol Conventions	. 7
1.5	Instruction Set Symbols	. 8

# 1.1 INTRODUCTION

Microchip Technology focuses on products for the embedded control market. Microchip is a leading supplier of the following devices and products:

- 8-bit General Purpose Microcontrollers (PIC<sup>®</sup> MCUs)
- 16-bit Digital Signal Controllers (dsPIC® DSCs)
- 16-bit and 32-bit Microcontrollers (MCUs)
- Speciality and Standard Nonvolatile Memory Devices
- Security Devices (KEELOQ<sup>®</sup> Security ICs)
- Application-specific Standard Products

Information about these devices and products, with corresponding technical documentation, is available on the Microchip web site (www.microchip.com).

## 1.2 MANUAL OBJECTIVE

This manual is a software developer's reference for the 16-bit MCU and DSC device families. It describes the Instruction Set in detail and also provides general information to assist the development of software for the 16-bit MCU and DSC device families.

This manual does not include detailed information about the core, peripherals, system integration or device-specific information. The user should refer to the specific device family reference manual for information about the core, peripherals and system integration. For device-specific information, the user should refer to the specific device data sheets. The information that can be found in the data sheets includes:

- Device memory map
- Device pinout and packaging details
- · Device electrical specifications
- · List of peripherals included on the device

Code examples are given throughout this manual. These examples are valid for any device in the 16-bit MCU and DSC families.

## 1.3 DEVELOPMENT SUPPORT

Microchip offers a wide range of development tools that allow users to efficiently develop and debug application code. Microchip's development tools can be broken down into four categories:

- Code generation
- Hardware/Software debug
- · Device programmer
- Product evaluation boards

Information about the latest tools, product briefs and user guides can be obtained from the Microchip web site (www.microchip.com) or from your local Microchip Sales Office.

Microchip offers other reference tools to speed the development cycle. These include:

- Application Notes
- · Reference Designs
- · Microchip web site
- · Local Sales Offices with Field Application Support
- Corporate Support Line

The Microchip web site also lists other sites that may be useful references.

# 1.4 STYLE AND SYMBOL CONVENTIONS

Throughout this document, certain style and font format conventions are used. Table 1-1 provides a description of the conventions used in this document.

Table 1-1:Document Conventions

Symbol or Term	Description
set	To force a bit/register to a value of logic '1'.
clear	To force a bit/register to a value of logic '0'.
Reset	1. To force a register/bit to its default state.
	<ol> <li>A condition in which the device places itself after a device Reset occurs. Some bits will be forced to '0' (such as interrupt enable bits), while others will be forced to '1' (such as the I/O data direction bits).</li> </ol>
0xnnnn	Designates the number 'nnnn' in the hexadecimal number system. These conventions are used in the code examples. For example, 0x013F or 0xA800.
: (colon)	Used to specify a range or the concatenation of registers/bits/pins. One example is ACCAU:ACCAH:ACCAL, which is the concatenation of three registers to form the 40-bit Accumulator. Concatenation order (left-right) usually specifies a positional relationship (MSb to LSb, higher to lower).
<>	Specifies bit locations in a particular register. One example is SR<7:5> (or IPL<2:0>), which specifies the register and associated bits or bit locations.
LSb, MSb	Indicates the Least Significant or Most Significant bit in a field.
LSB, MSB	Indicates the Least/Most Significant Byte in a field of bits.
lsw, msw	Indicates the least/most significant word in a field of bits
Courier New Font	Used for code examples, binary numbers and for Instruction mnemonics in the text.
Times New Roman Font, Italic	Used for equations and variables.
Times New Roman Font, Bold Italic	Used in explanatory text for items called out from a figure, equation, or example.
Note:	A Note presents information that we want to re-emphasize, either to help you avoid a common pitfall, or make you aware of operating differences between some device family members. A Note can be in a box, or when used in a table or figure, it is located at the bottom of the table or figure.

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# 1.5 INSTRUCTION SET SYMBOLS

The summary tables in Section 3.2 "Instruction Set Overview" and Section 7.2 "Instruction Set Summary Table", and the instruction descriptions in Section 5.4 "Instruction Descriptions" utilize the symbols shown in Table 1-2.

Table 1-2:	Symbols Used in Instruction Summary	<b>Tables and Descriptions</b>
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{ }       Optional field or operation         [text]       The location addressed by text         (text)       The contents of text         #text       The literal defined by text         a ∈ [b, c, d]       "a" must be in the set of [b, c, d]         cn:m>       Register bit field         {label:}       Optional label name         Accc       Accumulator A or Accumulator B         AWB       Accumulator Write Back         bit4       4-bit wide bit position (0:7 in Byte mode, 0:15 in Word mode)         Expr       Absolute address, label or expression (resolved by the linker)         f       File register address         lit1       1-bit literal (0:1)         lit2       4-bit literal (0:25)         lit1       1-bit literal (0:25)         lit14       4-bit literal (0:255)         lit15       5-bit literal (0:255 in Byte mode, 0:1023 in Word mode)         lit14       14-bit literal (0:255)         lit15       16-bit literal (0:6533)         lit12       12-bit literal (0:6535)         lit23       23-bit literal (-8:7)         Slit16       Signed 4-bit literal (-32:31) (range is limited to -16:16)         Slit16       Signed 10-bit literal (-32:768:32767)         TOS       Top-of-Stack <th>Symbol<sup>(1)</sup></th> <th>Description</th>	Symbol <sup>(1)</sup>	Description
(text)The contents of text#textThe literal defined by texta ∈ [b, c, d]"a" must be in the set of [b, c, d]cn:m>Register bit field{label1}Optional label nameAccAccumulator A or Accumulator BAWBAccumulator Write Backbit44-bit wide bit position (0:7 in Byte mode, 0:15 in Word mode)ExprAbsolute address, label or expression (resolved by the linker)fFile register address1it11-bit literal (0:1)1it44-bit literal (0:15)1it55-bit literal (0:25)1it1010-bit literal (0:255)1it1414-bit literal (0:255)1it1516-bit literal (0:255)1it1616-bit literal (0:6533)1it1712-bit literal (0:65535)1it2323-bit literal (0:8388607)S1it4Signed 4-bit literal (-32:31) (range is limited to -16:16)S1it10Signed 10-bit literal (-32:32) (range is limited to -16:16)S1it10Signed 10-bit literal (-32:768:32767)TOSTop-of-StackWbBase working register	{ }	Optional field or operation
#textThe literal defined by text $a \in [b, c, d]$ "a" must be in the set of $[b, c, d]$ $(n:m>$ Register bit field{label:}Optional label nameAccAccumulator A or Accumulator BAWBAccumulator Write Backbit44-bit wide bit position (0:7 in Byte mode, 0:15 in Word mode)ExprAbsolute address, label or expression (resolved by the linker)fFile register addresslit11-bit literal (0:1)lit44-bit literal (0:15)lit55-bit literal (0:25)lit6S-bit literal (0:25)lit1010-bit literal (0:255 in Byte mode, 0:1023 in Word mode)lit1414-bit literal (0:65535)lit1516-bit literal (0:65535)lit14Signed 4-bit literal (-8:7)Slit6Signed 6-bit literal (-32:31) (range is limited to -16:16)Slit10Signed 10-bit literal (-32768:32767)TOSTop-of-StackWbBase working register	[text]	The location addressed by text
$a \in [b, c, d]$ "a" must be in the set of $[b, c, d]$ <n:m>Register bit field{label:}Optional label nameAccAccumulator A or Accumulator BAWBAccumulator Write Backbit44-bit wide bit position (0:7 in Byte mode, 0:15 in Word mode)ExprAbsolute address, label or expression (resolved by the linker)fFile register addresslit11-bit literal (0:1)lit25-bit literal (0:15)lit55-bit literal (0:255)lit1010-bit literal (0:255)lit1414-bit literal (0:16383)lit1516-bit literal (0:6535)lit1414-bit literal (0:65535)lit15Signed 4-bit literal (-8:7)Slit6Signed 4-bit literal (-32:31) (range is limited to -16:16)slit10Signed 10-bit literal (-32:768:32767)TOSTop-of-StackWbBase working register</n:m>	(text)	The contents of text
<n:m>Register bit field{label:}Optional label nameAccAccumulator A or Accumulator BAWBAccumulator Write Backbit44-bit wide bit position (0:7 in Byte mode, 0:15 in Word mode)ExprAbsolute address, label or expression (resolved by the linker)fFile register addresslit11-bit literal (0:1)lit25-bit literal (0:15)lit55-bit literal (0:255)lit1010-bit literal (0:255 in Byte mode, 0:1023 in Word mode)lit1414-bit literal (0:65535)lit1616-bit literal (0:65535)lit2323-bit literal (-8:7)Slit6Signed 4-bit literal (-32:31) (range is limited to -16:16)Slit10Signed 10-bit literal (-32:768:32767)TOSTop-of-StackWbBase working register</n:m>	#text	The literal defined by text
{label:}Optional label nameAccAccumulator A or Accumulator BAWBAccumulator Write Backbit44-bit wide bit position (0:7 in Byte mode, 0:15 in Word mode)ExprAbsolute address, label or expression (resolved by the linker)fFile register addresslit11-bit literal (0:1)lit44-bit literal (0:15)lit55-bit literal (0:25)lit1010-bit literal (0:255)lit111-bit literal (0:255)lit1216-bit literal (0:6533)lit1414-bit literal (0:6535)lit2323-bit literal (0:8388607)Slit4Signed 4-bit literal (-8:7)Slit6Signed 10-bit literal (-32:31) (range is limited to -16:16)Slit10Signed 10-bit literal (-32:68:32767)TOSTop-of-StackWbBase working register	$a \in [b, c, d]$	"a" must be in the set of [b, c, d]
AccAccumulator A or Accumulator BAWBAccumulator Write Backbit44-bit wide bit position (0:7 in Byte mode, 0:15 in Word mode)ExprAbsolute address, label or expression (resolved by the linker)fFile register addresslit11-bit literal (0:1)lit44-bit literal (0:15)lit55-bit literal (0:31)lit88-bit literal (0:255)lit1010-bit literal (0:255 in Byte mode, 0:1023 in Word mode)lit1414-bit literal (0:6533)lit1616-bit literal (0:6535)lit2323-bit literal (0:65535)lit4Signed 4-bit literal (-32:31) (range is limited to -16:16)Slit10Signed 10-bit literal (-32768:32767)T0STop-of-StackWbBase working register	<n:m></n:m>	Register bit field
AWBAccumulator Write Backbit44-bit wide bit position (0:7 in Byte mode, 0:15 in Word mode)ExprAbsolute address, label or expression (resolved by the linker)fFile register address1it11-bit literal (0:1)1it44-bit literal (0:15)1it55-bit literal (0:31)1it88-bit literal (0:255)1it1010-bit literal (0:255 in Byte mode, 0:1023 in Word mode)1it1414-bit literal (0:65535)1it2323-bit literal (0:8388607)Slit4Signed 4-bit literal (-8:7)Slit6Signed 6-bit literal (-32:31) (range is limited to -16:16)Slit10Signed 10-bit literal (-32:768:32767)T0STop-of-StackWbBase working register	{label:}	Optional label name
bit44-bit wide bit position (0:7 in Byte mode, 0:15 in Word mode)ExprAbsolute address, label or expression (resolved by the linker)fFile register addresslit11-bit literal (0:1)lit44-bit literal (0:15)lit55-bit literal (0:31)lit88-bit literal (0:255)lit1010-bit literal (0:255 in Byte mode, 0:1023 in Word mode)lit1414-bit literal (0:65535)lit1616-bit literal (0:65535)lit2323-bit literal (0:8388607)Slit4Signed 4-bit literal (-8:7)Slit10Signed 10-bit literal (-32:31) (range is limited to -16:16)Slit110Signed 16-bit literal (-32768:32767)TOSTop-of-StackWbBase working register	Acc	Accumulator A or Accumulator B
Expr         Absolute address, label or expression (resolved by the linker)           f         File register address           1it1         1-bit literal (0:1)           1it4         4-bit literal (0:15)           1it5         5-bit literal (0:31)           1it8         8-bit literal (0:255)           1it10         10-bit literal (0:255 in Byte mode, 0:1023 in Word mode)           1it14         14-bit literal (0:65535)           1it16         16-bit literal (0:65535)           1it23         23-bit literal (0:8388607)           S1it4         Signed 4-bit literal (-32:31) (range is limited to -16:16)           S1it10         Signed 10-bit literal (-32:32) (range is limited to -16:16)           S1it10         Signed 16-bit literal (-32:767)           TOS         Top-of-Stack           Wb         Base working register	AWB	Accumulator Write Back
f       File register address         lit1       1-bit literal (0:1)         lit4       4-bit literal (0:15)         lit5       5-bit literal (0:31)         lit8       8-bit literal (0:255)         lit10       10-bit literal (0:255 in Byte mode, 0:1023 in Word mode)         lit14       14-bit literal (0:65535)         lit16       16-bit literal (0:65535)         lit23       23-bit literal (0:8388607)         Slit4       Signed 4-bit literal (-8:7)         Slit6       Signed 6-bit literal (-32:31) (range is limited to -16:16)         Slit10       Signed 16-bit literal (-512:511)         Slit16       Signed 16-bit literal (-32768:32767)         TOS       Top-of-Stack         Wb       Base working register	bit4	4-bit wide bit position (0:7 in Byte mode, 0:15 in Word mode)
lit1       1-bit literal (0:1)         lit4       4-bit literal (0:15)         lit5       5-bit literal (0:31)         lit8       8-bit literal (0:255)         lit10       10-bit literal (0:255 in Byte mode, 0:1023 in Word mode)         lit14       14-bit literal (0:16383)         lit16       16-bit literal (0:65535)         lit23       23-bit literal (0:8388607)         Slit4       Signed 4-bit literal (-8:7)         Slit6       Signed 6-bit literal (-32:31) (range is limited to -16:16)         Slit10       Signed 10-bit literal (-512:511)         Slit16       Signed 16-bit literal (-32768:32767)         TOS       Top-of-Stack         Wb       Base working register	Expr	Absolute address, label or expression (resolved by the linker)
lit4       4-bit literal (0:15)         lit5       5-bit literal (0:31)         lit8       8-bit literal (0:255)         lit10       10-bit literal (0:255 in Byte mode, 0:1023 in Word mode)         lit14       14-bit literal (0:16383)         lit16       16-bit literal (0:65535)         lit23       23-bit literal (0:8388607)         Slit4       Signed 4-bit literal (-8:7)         Slit6       Signed 6-bit literal (-32:31) (range is limited to -16:16)         Slit10       Signed 10-bit literal (-512:511)         Slit16       Signed 16-bit literal (-32768:32767)         T0S       Top-of-Stack         Wb       Base working register	f	File register address
1it5       5-bit literal (0:31)         1it8       8-bit literal (0:255)         1it10       10-bit literal (0:255 in Byte mode, 0:1023 in Word mode)         1it14       14-bit literal (0:16383)         1it16       16-bit literal (0:65535)         1it23       23-bit literal (0:8388607)         Slit4       Signed 4-bit literal (-8:7)         Slit6       Signed 6-bit literal (-32:31) (range is limited to -16:16)         Slit10       Signed 10-bit literal (-512:511)         Slit16       Signed 16-bit literal (-32768:32767)         T0S       Top-of-Stack         Wb       Base working register	lit1	1-bit literal (0:1)
lit8         8-bit literal (0:255)           lit10         10-bit literal (0:255 in Byte mode, 0:1023 in Word mode)           lit14         14-bit literal (0:16383)           lit16         16-bit literal (0:65535)           lit23         23-bit literal (0:8388607)           Slit4         Signed 4-bit literal (-8:7)           Slit6         Signed 6-bit literal (-32:31) (range is limited to -16:16)           Slit10         Signed 10-bit literal (-512:511)           Slit16         Signed 16-bit literal (-32768:32767)           TOS         Top-of-Stack           Wb         Base working register	lit4	4-bit literal (0:15)
lit10       10-bit literal (0:255 in Byte mode, 0:1023 in Word mode)         lit14       14-bit literal (0:16383)         lit16       16-bit literal (0:65535)         lit23       23-bit literal (0:8388607)         Slit4       Signed 4-bit literal (-8:7)         Slit6       Signed 6-bit literal (-32:31) (range is limited to -16:16)         Slit10       Signed 10-bit literal (-512:511)         Slit16       Signed 16-bit literal (-32768:32767)         TOS       Top-of-Stack         Wb       Base working register	lit5	5-bit literal (0:31)
lit14       14-bit literal (0:16383)         lit16       16-bit literal (0:65535)         lit23       23-bit literal (0:8388607)         Slit4       Signed 4-bit literal (-8:7)         Slit6       Signed 6-bit literal (-32:31) (range is limited to -16:16)         Slit10       Signed 10-bit literal (-512:511)         Slit16       Signed 16-bit literal (-32768:32767)         TOS       Top-of-Stack         Wb       Base working register	lit8	8-bit literal (0:255)
lit1616-bit literal (0:65535)lit2323-bit literal (0:8388607)Slit4Signed 4-bit literal (-8:7)Slit6Signed 6-bit literal (-32:31) (range is limited to -16:16)Slit10Signed 10-bit literal (-512:511)Slit16Signed 16-bit literal (-32768:32767)TOSTop-of-StackWbBase working register	lit10	10-bit literal (0:255 in Byte mode, 0:1023 in Word mode)
lit2323-bit literal (0:8388607)Slit4Signed 4-bit literal (-8:7)Slit6Signed 6-bit literal (-32:31) (range is limited to -16:16)Slit10Signed 10-bit literal (-512:511)Slit16Signed 16-bit literal (-32768:32767)TOSTop-of-StackWbBase working register	lit14	14-bit literal (0:16383)
Slit4Signed 4-bit literal (-8:7)Slit6Signed 6-bit literal (-32:31) (range is limited to -16:16)Slit10Signed 10-bit literal (-512:511)Slit16Signed 16-bit literal (-32768:32767)TOSTop-of-StackWbBase working register	lit16	16-bit literal (0:65535)
Slit6Signed 6-bit literal (-32:31) (range is limited to -16:16)Slit10Signed 10-bit literal (-512:511)Slit16Signed 16-bit literal (-32768:32767)TOSTop-of-StackWbBase working register	lit23	23-bit literal (0:8388607)
Slit10Signed 10-bit literal (-512:511)Slit16Signed 16-bit literal (-32768:32767)TOSTop-of-StackWbBase working register	Slit4	Signed 4-bit literal (-8:7)
Slit16Signed 16-bit literal (-32768:32767)TOSTop-of-StackWbBase working register	Slit6	Signed 6-bit literal (-32:31) (range is limited to -16:16)
TOS     Top-of-Stack       Wb     Base working register	Slit10	Signed 10-bit literal (-512:511)
Wb Base working register	Slit16	Signed 16-bit literal (-32768:32767)
	TOS	Top-of-Stack
	Wb	Base working register
Wd Destination working register (direct and indirect addressing)	Wd	Destination working register (direct and indirect addressing)
Wdo Destination working register (direct and indirect addressing, including indirect addressing with offs	Wdo	Destination working register (direct and indirect addressing, including indirect addressing with offset)
Wm, Wn         Working register divide pair (dividend, divisor)	Wm, Wn	Working register divide pair (dividend, divisor)
Wm * Wm         Working register multiplier pair (same source register)	Wm * Wm	Working register multiplier pair (same source register)
Wm * Wn Working register multiplier pair (different source registers)	Wm * Wn	Working register multiplier pair (different source registers)
Wn Both source and destination working register (direct addressing)	Wn	Both source and destination working register (direct addressing)
Wnd Destination working register (direct addressing)	Wnd	Destination working register (direct addressing)
Wns Source working register (direct addressing)	Wns	Source working register (direct addressing)
WREG Default working register (assigned to W0)	WREG	
Ws Source working register (direct and indirect addressing)	Ws	Source working register (direct and indirect addressing)
Wso Source working register (direct and indirect addressing, including indirect addressing with offset	Wso	Source working register (direct and indirect addressing, including indirect addressing with offset)
Wx         Source Addressing mode and working register for X data bus prefetch	W×	Source Addressing mode and working register for X data bus prefetch
Wxd Destination working register for X data bus prefetch	Wxd	Destination working register for X data bus prefetch
Wy         Source Addressing mode and working register for Y data bus prefetch	Wy	Source Addressing mode and working register for Y data bus prefetch
Wyd Destination working register for Y data bus prefetch	Wyd	Destination working register for Y data bus prefetch

**Note 1:** The range of each symbol is instruction dependent. Refer to **Section 5. "Instruction Descriptions**" for the specific instruction range.



# Section 2. Programmer's Model

# HIGHLIGHTS

This section of the manual contains the following major topics:

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2.2	Programmer's Model	14
2.3	Working Register Array	18
2.4	Default Working Register (WREG)	18
2.5	Software Stack Frame Pointer	18

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# 2.1 16-BIT MCU AND DSC CORE ARCHITECTURE OVERVIEW

This section provides an overview of the 16-bit architecture features and capabilities for the following families of devices:

- 16-bit Microcontrollers (MCU):
  - PIC24F
  - PIC24H
  - PIC24E
- 16-bit Digital Signal Controllers (DSC):
  - dsPIC30F
  - dsPIC33F
  - dsPIC33E

#### 2.1.1 Features Specific to 16-bit MCU and DSC Core

The core of the 16-bit MCU and DSC devices is a 16-bit (data) modified Harvard architecture with an enhanced instruction set. The core has a 24-bit instruction word, with an 8-bit Op code field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. An instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. The majority of instructions execute in a single cycle.

#### 2.1.1.1 REGISTERS

The 16-bit MCU and DSC devices have sixteen 16-bit working registers. Each of the working registers can act as a data, address or offset register. The 16th working register (W15) operates as a software Stack Pointer for interrupts and calls.

#### 2.1.1.2 INSTRUCTION SET

The instruction set is almost identical for the 16-bit MCU and DSC architectures. The instruction set includes many Addressing modes and was designed for optimum C compiler efficiency.

#### 2.1.1.3 DATA SPACE ADDRESSING

The data space can be addressed as 32K words or 64 Kbytes. The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary, which is a feature known as Program Space Visibility (PSV). The program to data space mapping feature lets any instruction access program space as if it were the data space, which is useful for storing data coefficients.

#### 2.1.1.4 ADDRESSING MODES

The core supports Inherent (no operand), Relative, Literal, Memory Direct, Register Direct, Register Indirect, and Register Offset Addressing modes. Each instruction is associated with a predefined Addressing mode group, depending upon its functional requirements. As many as seven Addressing modes are supported for each instruction.

For most instructions, the CPU is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, 3-operand instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

**Note:** Some devices families support Extended Data Space (EDS) addressing. See the specific device data sheet and family reference manual for more details on this feature.

#### 2.1.1.5 ARITHMETIC AND LOGIC UNIT

A high-speed, 17-bit by 17-bit multiplier is included to significantly enhance the core's arithmetic capability and throughput. The multiplier supports Signed, Unsigned, and Mixed modes, as well as 16-bit by 16-bit, or 8-bit by 8-bit integer multiplication. All multiply instructions execute in a single cycle.

The 16-bit Arithmetic Logic Unit (ALU) is enhanced with integer divide assist hardware that supports an iterative non-restoring divide algorithm. It operates in conjunction with the REPEAT instruction looping mechanism, and a selection of iterative divide instructions, to support 32-bit (or 16-bit) divided by 16-bit integer signed and unsigned division. All divide operations require 19 cycles to complete, but are interruptible at any cycle boundary.

#### 2.1.1.6 EXCEPTION PROCESSING

The 16-bit MCU and DSC devices have a vectored exception scheme with support for up to 8 sources of non-maskable traps and up to 246 interrupt sources. In both families, each interrupt source can be assigned to one of seven priority levels.

#### 2.1.2 PIC24E and dsPIC33E Features

In addition to the information provided in Section 2.1.1 "Features Specific to 16-bit MCU and DSC Core", this section describes the enhancements that are available in the PIC24E and dsPIC33E families of devices.

#### 2.1.2.1 DATA SPACE ADDRESSING

The Base Data Space address is used in conjunction with a read or write page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address, which can also be used for PSV access. The EDS can be addressed as 8 M words or 16 Mbytes. Refer to **Section 3. "Data Memory"** (DS70595) in the *"dsPIC33E/PIC24E Family Reference Manual"* for more details on EDS, PSV, and table accesses.

Note:	Some PIC24F devices also support Extended Data Space. Refer to Section 44.
	"CPU with EDS" (DS39732) and Section 45. "Data Memory with EDS"
	(DS39733) of the PIC24F Family Reference Manual for details.

#### 2.1.2.2 AUTOMATIC MIXED-SIGN MULTIPLICATION MODE (dsPIC33E ONLY)

In addition to signed and unsigned DSP multiplications, dsPIC33E devices support mixed-sign (unsigned-signed and signed-unsigned) multiplications without the need to dynamically reconfigure the multiplication mode and shift data to account for the difference in operand formats. This mode is particularly beneficial for executing extended-precision (32-bit and 64-bit) algorithms. Besides DSP instructions, MCU multiplication (MUL) instructions can also utilize either accumulator as a result destination, thereby enabling faster extended-precision arithmetic. Refer to 4.10.1 "Implied DSP Operands (dsPIC30F, dsPIC33F and dsPIC33E Devices)" and 4.18 "Extended-precision Arithmetic using mixed-sign multiplications (dsPIC33E only)" for more details on mixed-sign DSP multiplications.

#### 2.1.2.3 MCU MULTIPLICATIONS WITH 16-BIT RESULT

16x16-bit MUL instructions include an option to store the product in a single 16-bit working register rather than a pair of registers. This feature helps free up a register for other purposes, in cases where the numbers being multiplied are small in magnitude and therefore expected to provide a 16-bit result. See the individual MUL instruction descriptions in **5.4 "Instruction Descriptions"** for more details.

#### 2.1.2.4 HARDWARE STACK FOR DO LOOPS (dsPIC33E ONLY)

The single-level DO loop shadow register-set has been replaced by 4-level deep DO loop hardware stack. This provides automatic DO loop register save/restore for up to 3 levels of DO loop nesting, resulting in more efficient implementation of nested loops. Refer to 2.19 "DO Stack (dsPIC33E Devices)" for more details on DO loop nesting in dsPIC33E devices.

#### 2.1.2.5 DSP CONTEXT SWITCH SUPPORT (dsPIC33E ONLY)

In dsPIC33E devices, the DSP overflow and saturation status bits are writable. This allows the state of the DSP Engine to be efficiently saved and restored while switching between DSP tasks. See **2.16.4 "DSP ALU Status Bits (dsPIC30F, dsPIC33F and dsPIC33E Devices)**" for more details on DSP status bits.

#### 2.1.2.6 EXTENDED CALL AND GOTO INSTRUCTIONS

The new CALL.L Wn and GOTO.L Wn instructions extend the capabilities of the CALL Wn and GOTO Wn by enabling 32-bit addresses for computed branch/call destinations. In these enhanced instructions, the destination address is provided by a pair of working registers rather than a single 16-bit register. See the CALL.L and GOTO.L instruction descriptions in **5.4 "Instruction Descriptions"** for more details.

#### 2.1.2.7 COMPARE-BRANCH INSTRUCTIONS

dsPIC33E/PIC24E devices feature conditional Compare-Branch (CPBxx) instructions. These instructions extend the capabilities of the Compare-Skip (CPSxx) instructions by allowing branches rather than only skipping over a single instruction. See the CPBEQ, CPBNE, CPBGT and CPBLT instruction descriptions in **5.4 "Instruction Descriptions"** for more details on compare-branch instructions.

#### 2.1.3 dsPIC30F, dsPIC33F, and dsPIC33E Features

In addition to the information provided in Section 2.1.1 "Features Specific to 16-bit MCU and DSC Core", this section describes the DSP enhancements that are available in the dsPIC30F, dsPIC33F, and dsPIC33E families of devices.

#### 2.1.3.1 PROGRAMMING LOOP CONSTRUCTS

Overhead free program loop constructs are supported using the D0 instruction, which is interruptible.

#### 2.1.3.2 DSP INSTRUCTION CLASS

The DSP class of instructions.are seamlessly integrated into the architecture and execute from a single execution unit.

#### 2.1.3.3 DATA SPACE ADDRESSING

The data space is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operate solely through the X memory AGU, which accesses the entire memory map as one linear data space. The DSP dual source class of instructions operates through the X and Y AGUs, which splits the data address space into two parts. The X and Y data space boundary is arbitrary and device-specific.

#### 2.1.3.4 MODULO AND BIT-REVERSED ADDRESSING

Overhead-free circular buffers (modulo addressing) are supported in both X and Y address spaces. The modulo addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports bit-reverse addressing, to greatly simplify input or output data reordering for radix-2 FFT algorithms.

#### 2.1.3.5 DSP ENGINE

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value, up to 16 bits right, or up to 16 bits left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The MAC instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two working registers. This requires that

the data space be split for these instructions and linear for all others. This is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

#### 2.1.3.6 EXCEPTION PROCESSING

The dsPIC30F devices have a vectored exception scheme with support for up to 8 sources of non-maskable traps and up to 54 interrupt sources. The dsPIC33F and dsPIC33E have a similar exception scheme, but support up to 118, and up to 246 interrupt sources, respectively. In all three families, each interrupt source can be assigned to one of seven priority levels.

Refer to **Section 6** and **28** " **Interrupts**" of the dsPIC30F Family Reference Manual, **Sections 6, 29,32, 41, 47** and **53** of the dsPIC33F/PIC24H Family Reference Manual and **Section 6** of the dsPIC33E/PIC24E Family Reference Manual, for more details on Exception Processing.

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# 2.2 PROGRAMMER'S MODEL

Figure 2-1 through Figure 2-4 show the programmer's model diagrams for the 16-bit MCU and DSC families of devices.



#### Figure 2-1: PIC24F and PIC24H Programmer's Model Diagram



Figure 2-2: PIC24E Programmer's Model Diagram

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Programmer's Model







Figure 2-4: dsPIC33E Programmer's Model Diagram

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All registers in the programmer's model are memory mapped and can be manipulated directly by the instruction set. A description of each register is provided in Table 2-1.

Note: Unless otherwise specified, the Programmer's Model Register Descriptions in Table 2-1 apply to all MCU and DSC device families.

Register	Description		
CORCON	CPU Core Configuration register		
PC	23-bit Program Counter		
PSVPAG <sup>(1)</sup>	Program Space Visibility Page Address register		
DSRPAG <sup>(2)</sup>	Extended Data Space (EDS) Read Page register		
DSWPAG <sup>(2)</sup>	Extended Data Space (EDS) Write Page register		
RCOUNT	REPEAT Loop Count register		
SPLIM	Stack Pointer Limit Value register		
SR	ALU and DSP Engine STATUS register		
TBLPAG	Table Memory Page Address register		
W0-W15	Working register array		
ACCA, ACCB <sup>(3)</sup>	40-bit DSP Accumulators		
DCOUNT <sup>(3)</sup>	D0 Loop Count register		
DOSTART <sup>(3)</sup>	D0 Loop Start Address register		
DOEND <sup>(3)</sup>	D0 Loop End Address register		

Table 2-1: Programmer's Model Register Descriptions

**Note 1:** This register is only available on PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices.

- 2: This register is only available on PIC24E and dsPIC33E devices.
- 3: This register is only available on dsPIC30F, dsPIC33F, and dsPIC33E devices.

## 2.3 WORKING REGISTER ARRAY

The 16 working (W) registers can function as data, address or offset registers. The function of a W register is determined by the instruction that accesses it.

Byte instructions, which target the working register array, only affect the Least Significant Byte (LSB) of the target register. Since the working registers are memory mapped, the Least *and* Most Significant Bytes can be manipulated through byte-wide data memory space accesses.

# 2.4 DEFAULT WORKING REGISTER (WREG)

The instruction set can be divided into two instruction types: working register instructions and file register instructions. The working register instructions use the working register array as data values or as addresses that point to a memory location. In contrast, file register instructions operate on a specific memory address contained in the instruction opcode.

File register instructions that also utilize a working register do not specify the working register that is to be used for the instruction. Instead, a default working register (WREG) is used for these file register instructions. Working register, W0, is assigned to be the WREG. The WREG assignment is not programmable.

# 2.5 SOFTWARE STACK FRAME POINTER

A frame is a user-defined section of memory in the stack, used by a function to allocate memory for local variables. W14 has been assigned for use as a Stack Frame Pointer with the link (LNK) and unlink (ULNK) instructions. However, if a Stack Frame Pointer and the LNK and ULNK instructions are not used, W14 can be used by any instruction in the same manner as all other W registers. On dsPIC33E and PIC24E devices, a Stack Frame Active (SFA) Status bit is used to support nested stack frames. See Section 4.7.2 "Software Stack Frame Pointer" for detailed information about the Frame Pointer.

# 2.6 SOFTWARE STACK POINTER

W15 serves as a dedicated Software Stack Pointer, and will be automatically modified by function calls, exception processing and returns. However, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating the Stack Pointer. Refer to **Section 4.7.1 "Software Stack Pointer"** for detailed information about the Stack Pointer.

# 2.7 STACK POINTER LIMIT REGISTER (SPLIM)

The SPLIM is a 16-bit register associated with the Stack Pointer. It is used to prevent the Stack Pointer from overflowing and accessing memory beyond the user allocated region of stack memory. Refer to **Section 4.7.3 "Stack Pointer Overflow"** for detailed information about the SPLIM.

# 2.8 ACCUMULATOR A AND ACCUMULATOR B (dsPIC30F, dsPIC33F AND dsPIC33E DEVICES)

Accumulator A (ACCA) and Accumulator B (ACCB) are 40-bit wide registers, utilized by DSP instructions to perform mathematical and shifting operations. Each accumulator is composed of 3 memory mapped registers:

- AccxU (bits 39-32)
- AccxH (bits 31-16)
- AccxL (bits 15-0)

In dsPIC33E devices, Accumulator A and Accumulator B can also be used as destination registers in MCU MUL.xx instructions. This helps reduce the execution time of extended-precision arithmetic operations.

Refer to Section 4.12 "Accumulator Usage (dsPIC30F, dsPIC33F and dsPIC33E Devices)" for details on using ACCA and ACCB.

# 2.9 PROGRAM COUNTER

The Program Counter (PC) is 23 bits wide. Instructions are addressed in the 4M x 24-bit user program memory space by PC<22:1>, where PC<0> is always set to '0' to maintain instruction word alignment and provide compatibility with data space addressing. This means that during normal instruction execution, the PC increments by 2.

Program memory located at 0x800000 and above is utilized for device configuration data, Unit ID and Device ID. This region is not available for user code execution and the PC can not access this area. However, one may access this region of memory using table instructions. For details on accessing the configuration data, Unit ID, and Device ID, refer to the specific device family reference manual.

# 2.10 TBLPAG REGISTER

The TBLPAG register is used to hold the upper 8 bits of a program memory address during table read and write operations. Table instructions are used to transfer data between program memory space and data memory space. For details on accessing program memory with the table instructions, refer to the family reference manual of the specific device.

# 2.11 PSVPAG REGISTER (PIC24F, PIC24H, dsPIC30F AND dsPIC33F)

Program space visibility allows the user to map a 32-Kbyte section of the program memory space into the upper 32 Kbytes of data address space. This feature allows transparent access of constant data through instructions that operate on data memory. The PSVPAG register selects the 32-Kbyte region of program memory space that is mapped to the data address space. For details on program space visibility, refer to the specific device family reference manual.

# 2.12 RCOUNT REGISTER

The 14-bit RCOUNT register (16-bit for PIC24E and dsPIC33E devices) register contains the loop counter for the REPEAT instruction. When a REPEAT instruction is executed, RCOUNT is loaded with the repeat count of the instruction, either "lit14" for the "REPEAT #lit14" instruction ("lit15" for the "REPEAT #lit15" instruction for PIC24E and dsPIC33E devices), or the 14 LSb of the Wn register for the "REPEAT Wn" instruction (entire Wn for PIC24E and dsPIC33E devices). The REPEAT loop will be executed RCOUNT + 1 time.

- **Note 1:** If a REPEAT loop is executing and gets interrupted, RCOUNT may be cleared by the Interrupt Service Routine to break out of the REPEAT loop when the foreground code is re-entered.
  - 2: Refer to the specific device family reference manual for complete details about REPEAT loops.

## 2.13 DCOUNT REGISTER (dsPIC30F, dsPIC33F AND dsPIC33E DEVICES)

The 14-bit DCOUNT register (16-bit for dsPIC33E devices) contains the loop counter for hardware D0 loops. When a D0 instruction is executed, DCOUNT is loaded with the loop count of the instruction, either "lit14" for the "D0 #lit14, Expr" instruction ("lit15" for the "D0 #lit15, Expr" instruction for dsPIC33E devices) or the 14 LSb of the Ws register for the "D0 Ws, Expr" instruction (entire Wn for dsPIC33E devices). The D0 loop will be executed DCOUNT + 1 times.

- **Note 1:** In dsPIC30F and dsPIC33F devices, the DCOUNT register contains a shadow register. See Section 2.18 "Shadow Registers" for information on shadow registers.
  - The dsPIC33E devices have a 4-level-deep, nested D0 stack instead of a shadow register.
  - **3:** Refer to the specific device family reference manual for complete details about D0 loops.

## 2.14 DOSTART REGISTER (dsPIC30F, dsPIC33F AND dsPIC33E DEVICES)

The DOSTART register contains the starting address for a hardware D0 loop. When a D0 instruction is executed, DOSTART is loaded with the address of the instruction that follows the D0 instruction. This location in memory is the start of the D0 loop. When looping is activated, program execution continues with the instruction stored at the DOSTART address after the last instruction in the D0 loop is executed. This mechanism allows for zero overhead looping.

- Note 1: For dsPIC30F and dsPIC33F devices, DOSTART has a shadow register. See Section 2.18 "Shadow Registers" for information on shadowing.
  - 2: The dsPIC33E devices have a 4-level-deep, nested D0 stack instead of a shadow register. The DOSTART register is read-only in dsPIC33E devices.
  - **3:** Refer to the specific device family reference manual for complete details about D0 loops.

# 2.15 DOEND REGISTER (dsPIC30F, dsPIC33F AND dsPIC33E DEVICES)

The DOEND register contains the ending address for a hardware D0 loop. When a D0 instruction is executed, DOEND is loaded with the address specified by the expression in the D0 instruction. This location in memory specifies the last instruction in the D0 loop. When looping is activated and the instruction stored at the DOEND address is executed, program execution will continue from the D0 loop start address (stored in the DOSTART register).

- Note 1: For dsPIC30F and dsPIC33F devices, DOEND has a shadow register. See Section 2.18 "Shadow Registers" for information on shadow registers.
  - 2: The dsPIC33E devices have a 4-level-deep, nested D0 stack instead of a shadow register.
  - **3:** Refer to the specific device family reference manual for complete details about D0 loops.

## 2.16 STATUS REGISTER

The 16-bit STATUS register maintains status information for the instructions which have been executed most recently. Operation Status bits exist for MCU operations, loop operations and DSP operations. Additionally, the STATUS register contains the CPU Interrupt Priority Level bits, IPL<2:0>, which are used for interrupt processing.

Depending on the MCU and DSC family, one of the following STATUS registers is used:

- Register 2-1 for PIC24F, PIC24H, and PIC24E devices
- Register 2-2 for dsPIC30F and dsPIC33F devices
- Register 2-3 for dsPIC33E devices

#### 2.16.1 MCU ALU Status Bits

The MCU operation Status bits are either affected or used by the majority of instructions in the instruction set. Most of the logic, math, rotate/shift and bit instructions modify the MCU Status bits after execution, and the conditional Branch instructions use the state of individual Status bits to determine the flow of program execution. All conditional branch instructions are listed in **Section 4.8 "Conditional Branch Instructions"**.

The Carry (C), Zero (Z), Overflow (OV), Negative (N), and Digit Carry (DC) bits show the immediate status of the MCU ALU by indicating whether an operation has resulted in a Carry, Zero, Overflow, <u>Negative</u> result, or Digit Carry. When a subtract operation is performed, the C flag is used as a Borrow flag.

The Z Status bit is useful for extended precision arithmetic. The Z Status bit functions like a normal Z flag for all instructions except those that use a carry or borrow input (ADDC, CPB, SUBB and SUBBR). See Section 4.9 "Z Status Bit" for more detailed information.

- **Note 1:** All MCU bits are shadowed during execution of the PUSH. S instruction and they are restored on execution of the POP. S instruction.
  - **2:** All MCU bits, except the DC flag (which is not in the SRL), are stacked during exception processing (see **Section 4.7.1 "Software Stack Pointer**").

#### 2.16.2 REPEAT Loop Status Bit

The REPEAT Active bit (RA) is used to indicate when looping is active. The RA flag indicates that a REPEAT instruction is being executed, and it is only affected by the REPEAT instructions. The RA flag is set to '1' when the instruction being repeated begins execution, and it is cleared when the instruction being repeated completes execution for the last time.

Since the RA flag is also read-only, it may not be directly cleared. However, if a REPEAT or its target instruction is interrupted, the Interrupt Service Routine may clear the RA flag of the SRL, which resides on the stack. This action will disable looping once program execution returns from the Interrupt Service Routine, because the restored RA will be '0'.

Programmer's

Mode

### 2.16.3 DO Active bit (DA) (dsPIC30F, dsPIC33F and dsPIC33E Devices)

The DO Active bit (DA) is used to indicate when looping is active. The D0 instructions affect the DA flag, which indicates that a D0 loop is active. The DA flag is set to '1' when the first instruction of the D0 loop is executed, and it is cleared when the last instruction of the loop completes final execution.

The DA flag is read-only. This means that looping is not initiated by writing a '1' to DA, nor is it terminated by writing a '0' to DA. If a D0 loop must be terminated prematurely, the EDT bit, CORCON<11>, should be used.

# 2.16.4 DSP ALU Status Bits (dsPIC30F, dsPIC33F and dsPIC33E Devices)

The high byte of the STATUS Register (SRH) is used by the DSP class of instructions, and it is modified when data passes through one of the adders. The SRH provides status information about overflow and saturation for both accumulators. The Saturate A, Saturate B, Overflow A and Overflow B (SA, SB, OA, OB) bits provide individual accumulator status, while the Saturate AB and Overflow AB (SAB, OAB) bits provide combined accumulator status. The SAB and OAB bits provide an efficient method for the software developer to check the register for saturation or overflow.

The OA and OB bits are used to indicate when an operation has generated an overflow into the guard bits (bits 32 through 39) of the respective accumulator. This condition can only occur when the processor is in Super Saturation mode, or if saturation is disabled. It indicates that the operation has generated a number which cannot be represented with the lower 31 bits of the accumulator. The OA and OB bits are writable in dsPIC33E devices.

The SA and SB bits are used to indicate when an operation has generated an overflow out of the MSb of the respective accumulator. The SA and SB bits are active, regardless of the Saturation mode (Disabled, Normal or Super) and may be considered "sticky". Namely, once the SA or SB bit is set to '1', it can only be cleared manually by software, regardless of subsequent DSP operations. When it is required, the BCLR instruction can be used to clear the SA or SB bit.

In addition, the SA and SB bits can be set by software in dsPIC33E devices, enabling efficient context state switching.

For convenience, the OA and OB bits are logically ORed together to form the OAB flag, and the SA and SB bits are logically ORed to form the SAB flag. These cumulative Status bits provide efficient overflow and saturation checking when an algorithm is implemented. Instead of interrogating the OA and the OB bits independently for arithmetic overflows, a single check of OAB can be performed. Likewise, when checking for saturation, SAB may be examined instead of checking both the SA and SB bits. Note that clearing the SAB flag will clear both the SA and SB bits.

#### 2.16.5 Interrupt Priority Level Status Bits

The three Interrupt Priority Level (IPL) bits of the SRL, SR<7:5>, and the IPL3 bit, CORCON<3>, set the CPU's IPL which is used for exception processing. Exceptions consist of interrupts and hardware traps. Interrupts have a user-defined priority level between 0 and 7, while traps have a fixed priority level between 8 and 15. The fourth Interrupt Priority Level bit, IPL3, is a special IPL bit that may only be read or cleared by the user. This bit is only set when a hardware trap is activated and it is cleared after the trap is serviced.

The CPU's IPL identifies the lowest level exception which may interrupt the processor. The interrupt level of a pending exception must always be greater than the CPU's IPL for the CPU to process the exception. This means that if the IPL is 0, all exceptions at priority Level 1 and above may interrupt the processor. If the IPL is 7, only hardware traps may interrupt the processor.

When an exception is serviced, the IPL is automatically set to the priority level of the exception being serviced, which will disable all exceptions of equal and lower priority. However, since the IPL field is read/write, one may modify the lower three bits of the IPL in an Interrupt Service Routine to control which exceptions may preempt the exception processing. Since the SRL is stacked during exception processing, the original IPL is always restored after the exception is serviced. If required, one may also prevent exceptions from nesting by setting the NSTDIS bit (INTCON1<15>).

**Note:** For more detailed information on exception processing, refer to the family reference manual of the specific device.

# 2.17 CORE CONTROL REGISTER

For all MCU and DSC devices, the 16-bit CPU Core Control register (CORCON), is used to set the configuration of the CPU. This register provides the ability to map program space into data space.

In addition to setting CPU modes, the CORCON register contains status information about the IPL<3> Status bit, which indicates if a trap exception is being processed.

Depending on the MCU and DSC family, one of the following CORCON registers is used:

- Register 2-4 for PIC24F and PIC24H devices
- Register 2-5 for PIC24E devices
- Register 2-6 for dsPIC30F and dsPIC33F devices
- Register 2-7 for dsPIC33E devices

### 2.17.1 dsPIC30F, dsPIC33F, and dsPIC33E Specific bits

In addition to setting CPU modes, the following features are available through the CORCON register:

- Set the ACCA and ACCB saturation enable
- Set the Data Space Write Saturation mode
- Set the Accumulator Saturation and Rounding modes
- Set the Multiplier mode for DSP operations
- Terminate D0 loops prematurely
- Provide status information about the D0 loop nesting level (DL<2:0>)
- Select fixed or variable interrupt latency (dsPIC33E only)

#### 2.17.1.1 PIC24E and dsPIC33E SPECIFIC BITS

A Status bit (SFA) is available that indicates whether the Stack Frame is active.

Note: PIC24E and dsPIC33E devices do not have a PSV control bit, it has been replaced by the SFA bit.

## 2.18 SHADOW REGISTERS

A shadow register is used as a temporary holding register and can transfer its contents to or from the associated host register when instructed. Some of the registers in the programmer's model have a shadow register, which is utilized during the execution of a D0, POP.S, or PUSH.S instruction. Shadow register usage is shown in Table 2-2.

Note: The D0 instruction is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.

#### Table 2-2: Automatic Shadow Register Usage

Location	D0 <sup>(1)</sup>	POP.S/PUSH.S
DCOUNT <sup>(1)</sup>	Yes	_
DOSTART <sup>(1)</sup>	Yes	—
DOEND <sup>(1)</sup>	Yes	—
STATUS Register – DC, N, OV, Z and C bits	—	Yes
W0-W3		Yes

Note 1: The D0 shadow registers are only available in dsPIC30F and dsPIC33F devices.

For dsPIC30F and dsPIC33F devices, since the DCOUNT, DOSTART and DOEND registers are shadowed, the ability to nest D0 loops without additional overhead is provided. Since all shadow registers are one register deep, up to one level of D0 loop nesting is possible. Further nesting of D0 loops is possible in software, with support provided by the D0 Loop Nesting Level Status bits (DL<2:0>) in the CORCON register (CORCON<10:8>).

**Note:** All shadow registers are one register deep and not directly accessible. Additional shadowing may be performed in software using the software stack.

# 2.19 DO STACK (dsPIC33E DEVICES)

The DO stack is used to preserve the following elements associated with a D0 loop underway when another D0 loop is encountered (i.e., a nested D0 loop).

- DOSTART register value
- DOEND register value
- DCOUNT register value

Note that the DO level status field (DL<2:0>) also acts as a pointer to address the DO stack. After the D0 instruction is executed, the DO level status field (DL<2:0>) points to the next free entry.

The DOSTART, DOEND, and DCOUNT registers each have an associated hardware stack that allows the D0 loop hardware to support up to three levels of nesting. A conceptual representation of the D0 stack is shown in Figure 2-5.

Figure 2-5: DO Stack Conceptual Diagram



Programmer's

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0			
	_	—	_	—		—	DC			
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0			
IPL2 <sup>(1,2)</sup>	IPL1 <sup>(1,2)</sup>	IPL0 <sup>(1,2)</sup>	RA	N	OV	Z	С			
bit 7							bit			
Legend:				U = Unimpler	nented bit, read	d as '0'				
R = Readal	ole bit	W = Writable	bit	C = Clearable						
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	iown			
bit 15-9	-	ted: Read as '								
bit 8		U Half Carry/Bo								
		ut from the 4th	low order bit	tor byte-sized d	iata) or 8th Iow	order bit (for wo	ord-sized data			
			low order bit	(for byte-sized	data) or 8th low	order bit (for wo	ord-sized dat			
		ult occurred		<i></i>						
oit 7-5		PU Interrupt Pri								
		111 = CPU Interrupt Priority Level is 7 (15). User interrupts disabled 110 = CPU Interrupt Priority Level is 6 (14)								
		110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13)								
	100 = CPU Ir	100 = CPU Interrupt Priority Level is 4 (12)								
		011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10)								
		nterrupt Priority								
		nterrupt Priority								
bit 4	RA: REPEAT	Loop Active bit								
	1 = REPEAT loop in progr									
	0 = REPEAT loop not in progress									
bit 3	N: MCU ALU	0								
	1 = Result wa 0 = Result wa	as negative as non-negative	e (zero or pos	itive)						
bit 2		U Overflow bit	. (							
			rithmetic (2's	complement). It	indicates an o	verflow of the m	nagnitude tha			
		gn bit to chang								
	1 = Overflow 0 = No overfl		gned arithme	tic (in this arithn	netic operation)	)				
bit 1	Z: MCU ALU									
		= An operation that affects the Z bit has set it at some time in the past								
						a non-zero resul	t)			
bit 0		Carry/Borrow								
		ut from the MS								
	$\Theta = NO carry-$	out from the M	SD occurred							
Note 1:	The IPL<2:0> bits	are concatenat	ted with the II	PL3 bit (CORCO	DN<3>) to form	the CPU Interr	upt Prioritv			
	Level. The value i									
	PL<3> = 1.									
2.	The IPL<2:0> Stat	ue hite are read	t only whon t		INTOONIA -1ES					

**2:** The IPL<2:0> Status bits are read only when the NSTDIS bit (INTCON1<15>) = 1. Refer to the family reference manual of the specific device family to see the associated interrupt register.

R-0	R-0	R/C-0	R/C-0	R-0	R/C-0	R-0	R/W-0
OA	OB	SA <sup>(1,2)</sup>	SB <sup>(1,2)</sup>	OAB	SAB <sup>(1,2,3)</sup>	DA <sup>(4)</sup>	DC
oit 15							bi
R/W-0		R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2 <sup>(5</sup>	) IPL1 <sup>(5)</sup>	IPL0 <sup>(5)</sup>	RA	N	OV	Z	C
bit 7							bi
Legend:							
R = Reada	able bit	W = Writable	bit	C = Clearabl	e bit		
-n = Value	at POR	'1' = Bit is set	:	'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15		lator A Overflo					
		ator A overflow					
hi+ 1 /		ator A has not					
bit 14		Ilator B Overflo ator B overflow					
		ator B has not					
bit 13	SA: Accumu	lator A Saturati	on bit <b>(1, 2)</b>				
				en saturated si	nce this bit was	last cleared	
		ator A is not sa					
bit 12		lator B Saturati			t ainaa thia hit w		
		ator B is satura ator B is not sa		en saluraleo a	t since this bit wa	as last cleared	
bit 11		OB Combined /		verflow bit			
		ator A or B has					
		Accumulator A					
bit 10		B Combined A					
		ator A or B is s Accumulator A i			ed since this bit	was last cleare	d
bit 9	DA: D0 Loop		ioi o is satula				
UIL J	1 = D0 loop i						
		not in progress					
bit 8	DC: MCU AL	U Half Carry b	it				
		out from the MS					
		-out from the M		er nibble occur	red		
bit 7-5		terrupt Priority nterrupt Priority		5) Llear interru	inte disabled		
		nterrupt Priority			ipis disabled		
		nterrupt Priority					
		nterrupt Priority	•	,			
		nterrupt Priority nterrupt Priority	· · · ·	,			
		nterrupt Priority					
		nterrupt Priority					
Note 1-	This hit may be re	ad or closed	but not cot				
Note 1: 2:	This bit may be re Once this bit is se			/ hv/software			
3:	Clearing this bit w			by sollward.			
3. 4:	This bit is read-on						
4. 5:	The IPL<2:0> bits	-	ted with the IP	L3 bit (CORC)	ON<3>) to form	the CPU Intern	upt Priority
0.	Level. The value i						

2

Register 2-2:	SR: CPU STATUS Register (dsPIC30F and dsPIC33F Devices) (Continued)
bit 4	<ul> <li>RA: REPEAT Loop Active bit</li> <li>1 = REPEAT loop in progress</li> <li>0 = REPEAT loop not in progress</li> </ul>
bit 3	<ul> <li>N: MCU ALU Negative bit</li> <li>1 = The result of the operation was negative</li> <li>0 = The result of the operation was not negative</li> </ul>
bit 2	<ul> <li>OV: MCU ALU Overflow bit</li> <li>1 = Overflow occurred</li> <li>0 = No overflow occurred</li> </ul>
bit 1	<ul> <li>Z: MCU ALU Zero bit</li> <li>1 = The result of the operation was zero</li> <li>0 = The result of the operation was not zero</li> </ul>
bit 0	<b>C:</b> MCU ALU Carry/Borrow bit 1 = A carry-out from the MSb occurred 0 = No carry-out from the MSb occurred

- Note 1: This bit may be read or cleared, but not set.
  - **2:** Once this bit is set, it must be cleared manually by software.
  - **3:** Clearing this bit will clear SA and SB.
  - 4: This bit is read-only.
  - **5:** The IPL<2:0> bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL3 = 1.

OB R/W-0 IPL1 <sup>(1,2)</sup>	R/W-0	SB <sup>(3)</sup>	OAB	SAB	DA	DC bit	
		R-0				bit	
		R-0	<b>D N U O</b>				
		R-0	-				
IPL1 <sup>(1,2)</sup>	$1 = 1 \circ (12)$		R/W-0	R/W-0	R/W-0	R/W-0	
	IPL0(-,-)	RA	N	OV	Z	С	
						bit	
					(0)		
			•	nented bit, read	as '0'		
POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	IOWN	
1 = Accumula	ator A has overf	lowed					
1 = Accumula	ator B has overf	lowed					
1 = Accumula	ator A is saturate	ed or has bee	n saturated sir	nce this bit was	last cleared		
1 = Accumula	ator B is saturate	ed or has bee	n saturated sir	nce this bit was	last cleared		
1 = Accumula	ator A or B has (	overflowed		bit			
1 = Accumula	ator A or B is sa	turated or has	s been saturate	ed since this bit	was last cleare	ed	
1 = D0 loop ii	n progress						
1 = A carry-o of the res 0 = No carry-	ut from the 4th I ult occurred out from the 4th	ow order bit (f	-				
	1 = Accumula 0 = Accumula 0 = Accumula 0 = Accumula 0 = Accumula 1 = Accumula 0 = Accumula 1 = Accumula 0 = Neither A DA: DO Loopp 1 = DO loop ri 0 = DO loop ri 0 = DO loop ri 0 = DO loop ri 0 = No carry-o o f the res 0 = No carry-	OR '1' = Bit is set OA: Accumulator A Overflow 1 = Accumulator A has overf 0 = Accumulator A has not o OB: Accumulator B Overflow 1 = Accumulator B has not o SA: Accumulator B has not o SA: Accumulator A Saturatio 1 = Accumulator A Saturatio 1 = Accumulator A Saturatio 1 = Accumulator A is saturatio 1 = Accumulator B Saturatio 1 = Accumulator B is saturatio 1 = Accumulator B is not saturatio 1 = Accumulator A or B has o 0 = Neither Accumulator A no SAB: SA    SB Combined Act 1 = Accumulator A or B is saturation 0 = Neither Accumulator A no SAB: SA    SB Combined Act 1 = Accumulator A or B is saturation 0 = Neither Accumulator A no DA: D0 Loop Active bit 1 = D0 loop not in progress 0 = D0 loop not in progress DC: MCU ALU Half Carry/Bo 1 = A carry-out from the 4th I of the result occurred	OR       '1' = Bit is set         OA: Accumulator A Overflow Status bit       1 = Accumulator A has overflowed         0 = Accumulator A has not overflowed       0 = Accumulator B Overflow Status bit         1 = Accumulator B has not overflowed       0 = Accumulator B has overflowed         0 = Accumulator B has not overflowed       0 = Accumulator B has not overflowed         SA: Accumulator A saturation Status bit       1 = Accumulator A is saturated or has bee         0 = Accumulator A is not saturated       SB: Accumulator B Saturation Status bit         1 = Accumulator B is saturated or has bee       0 = Accumulator B is not saturated         SB: Accumulator B is not saturated       OAB: OA    OB Combined Accumulator Of         1 = Accumulator A or B has overflowed       0 = Neither Accumulator A nor B has overflowed         0 = Neither Accumulator A or B is saturated or has       0 = Neither Accumulator A nor B has overflowed         0 = Neither Accumulator A or B is saturated or has       0 = Neither Accumulator A nor B is saturated         DA: D0 Loop Active bit       1 = D0 loop in progress         0 = D0 loop not in progress       0 = D0 loop not in progress         DC: MCU ALU Half Carry/Borrow bit       1 = A carry-out from the 4th low order bit (for the result occurred         0 = No carry-out from the 4th low order bit (for the result occurred       0 = No carry-out from the 4th low order bit (for the result occurred	bitW = Writable bitC = ClearablePOR'1' = Bit is set'0' = Bit is cleOA: Accumulator A Overflow Status bit1 = Accumulator A has overflowed0 = Accumulator A has not overflowed0B: Accumulator B Overflow Status bit1 = Accumulator B has overflowed0 = Accumulator B has overflowed0 = Accumulator A Saturation Status bit1 = Accumulator A Saturation Status bit1 = Accumulator A is saturated or has been saturated sir0 = Accumulator A is not saturatedSB: Accumulator B Saturation Status bit1 = Accumulator B is saturated or has been saturated sir0 = Accumulator B is not saturatedSB: Accumulator B is not saturatedOAB: OA    OB Combined Accumulator Overflow Status1 = Accumulator A or B has overflowed0 = Neither Accumulator A nor B has overflowed0 = Neither Accumulator A nor B has overflowed0 = Neither Accumulator A nor B is saturatedDA: D0 Loop Active bit1 = D0 loop in progress0 = D0 loop not in progressDC: MCU ALU Half Carry/Borrow bit1 = A carry-out from the 4th low order bit (for byte-sized or of the result occurred0 = No carry-out from the 4th low order bit (for byte-sized or of the result occurred	bit       W = Writable bit       C = Clearable bit         POR       '1' = Bit is set       '0' = Bit is cleared         OA: Accumulator A Overflow Status bit       1 = Accumulator A has overflowed       0 = Bit is cleared         OB: Accumulator A has not overflowed       0 = Accumulator B has overflowed       0         OB: Accumulator B Overflow Status bit       1 = Accumulator B has overflowed       0         0 = Accumulator B has overflowed       0 = Accumulator A saturation Status bit       1 = Accumulator A Saturation Status bit         1 = Accumulator A is not saturated or has been saturated since this bit was       0 = Accumulator B is not saturated         SB: Accumulator B Saturation Status bit       1 = Accumulator B is not saturated         SB: Accumulator B Saturated or has been saturated since this bit was       0 = Accumulator B is not saturated         OAB: OA    OB Combined Accumulator Overflow Status bit       1 = Accumulator A or B has overflowed         0 = Neither Accumulator A nor B has overflowed       SAB: SA    SB Combined Accumulator Status bit         1 = Accumulator A or B is saturated or has been saturated since this bit bit       0 = Neither Accumulator A nor B is saturated         DA: D0 Loop Active bit       1 = D0 loop in progress       0 = D0 loop not in progress         0 = D0 loop not in progress       DC: MCU ALU Half Carry/Borrow bit       1 = A carry-out from the 4th low order bit (for byte-sized data) or 8th low of	bit       W = Writable bit       C = Clearable bit         POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         OA: Accumulator A Overflow Status bit       1 = Accumulator A has overflowed       0 = Bit is cleared       x = Bit is unknown         OB: Accumulator A has not overflowed       0 = Accumulator A has not overflowed       0         OB: Accumulator B Overflow Status bit       1 = Accumulator B has overflowed       0         0 = Accumulator A Saturation Status bit       1 = Accumulator A is sot overflowed       0         SA: Accumulator A Saturation Status bit       1 = Accumulator A is not saturated       0         Accumulator B Saturated or has been saturated since this bit was last cleared       0         0 = Accumulator B is not saturated       0         SB: Accumulator B is not saturated       0         OAB: OA    OB Combined Accumulator Overflow Status bit       1 = Accumulator A or B has overflowed         0 = Neither Accumulator A nor B has overflowed       0 = Neither Accumulator A nor B has overflowed         0 = Neither Accumulator A nor B is saturated       0         DAB: DA    SB Combined Accumulator Status bit       1 = Accumulator A or B is saturated or has been saturated since this bit was last cleared         0 = Neither Accumulator A nor B is saturated       DA: DO Loop Active bit       1 = DO loop not in progress         <	

**3:** A data write to SR can modify the SA or SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA/SB bit write race-condition, the SA and SB bits should not be modified using bit operations.

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Register 2-3:	SR: CPU STATUS Register (dsPIC33E Devices) (Continued)
bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits <sup>(1,2)</sup> 111 = CPU Interrupt Priority Level is 7 (15). User interrupts disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8)
bit 4	<ul> <li>RA: REPEAT Loop Active bit</li> <li>1 = REPEAT loop in progress</li> <li>0 = REPEAT loop not in progress</li> </ul>
bit 3	<ul> <li>N: MCU ALU Negative bit</li> <li>1 = Result was negative</li> <li>0 = Result was non-negative (zero or positive)</li> </ul>
bit 2	<ul> <li>OV: MCU ALU Overflow bit</li> <li>This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state.</li> <li>1 = Overflow occurred for signed arithmetic (in this arithmetic operation)</li> <li>0 = No overflow occurred</li> </ul>
bit 1	<ul> <li>Z: MCU ALU Zero bit</li> <li>1 = The result of the operation was zero</li> <li>0 = The result of the operation was not zero</li> </ul>
bit 0	<b>C:</b> MCU ALU Carry/Borrow bit 1 = A carry-out from the MSb of the result occurred 0 = No carry-out from the MSb of the result occurred
Noto 1. Th	$\alpha$ IPL < 2:0\ hits are consistent with the IPL 2 hit (COPCON<2\) to form the CPL Latercust Priority

- **Note 1:** The IPL<2:0> bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL3 = 1. User interrupts are disabled when IPL3 = 1.
  - **2:** The IPL<2:0> Status bits are read only when NSTDIS bit (INTCON1<15>) = 1. Refer to the family reference manual of the specific device family to see the associated interrupt register.
  - **3:** A data write to SR can modify the SA or SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA/SB bit write race-condition, the SA and SB bits should not be modified using bit operations.

Register 2-4:	CORCON: 0	Core Control F	CORCON: Core Control Register (PIC24F and PIC24H Devices)				
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—				_	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R/C-0	R/W-0	U-0	U-0
—			_	IPL3 <sup>(1,2)</sup>	PSV	—	—
bit 7							bit 0
Legend:	C = Clearable bit		e bit	R = Readabl	e bit	W = Writable	bit
-n = Value at POR '1' =		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
U = Unimpleme	ented bit, read	as '0'					
bit 15-4 bit 3 bit 2	<b>IPL3:</b> Interrup 1 = CPU Inter 0 = CPU Inter <b>PSV:</b> Program	rrupt Priority Le n Space Visibil	l 3 Status bit <sup>(1,</sup> evel is 8 or gre evel is 7 or les ity in Data Spa	ater (trap exce s (no trap exce	eption activated) eption activated)		
	5	1 = Program space visible in data space 0 = Program space not visible in data space					

bit 1-0 Unimplemented: Read as '0'

Note 1: This bit may be read or cleared, but not set.

2: This bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

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# 16-bit MCU and DSC Programmer's Reference Manual

Register 2-5:	CORCON: (	Core Control F	Register (PIC	24E Devices)			
R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
VAR		—	_	_	—	_	_
bit 15							bit 8
U-0	U-0	U-0	U-0	R/C-0	R-0	U-0	U-0
	_		_	IPL3 <sup>(1,2)</sup>	SFA		_
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown			iown	
bit 15	VAR: Variable	e Exception Pro	cessing Later	ncy Control bit			
	· · · · · ·	bounded detern	, ,	•	0 2		
	<ul> <li>0 = Fixed (fully deterministic) exception processing latency</li> <li>Unimplemented: Read as '0'</li> </ul>						
bit 3	IPL3: CPU In	terrupt Priority	Level Status b	oit 3 <sup>(1)</sup>			
:	1 = CPU inter	rupt priority lev	el is greater tl	nan 7			
	0 = CPU inter	rupt priority lev	el is 7 or less				
				address 0x00	000 to 0xFFFF,	regardless of	DSRPAG and
			. W14 and W1	15 address of I	EDS or Base Da	ata Space	
		ted: Read as '0				·	
	•						

- Note 1: This bit may be read or cleared, but not set.
  - 2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

U-0	U-0	U-0	R/W-0	R(0)/W-0	R-0	R-0	R-0
_	_	_	US	EDT <sup>(1)</sup>		DL<2:0> <sup>(2,3)</sup>	
bit 15							bit
544.0	54440	50000		<b>D</b> /2.2	5444	5444.0	
R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0
SATA bit 7	SATB	SATDW	ACCSAT	IPL3(4,0)	PSV	RND	IF bit
							DIL
Legend:		C = Clearabl	e bit	R = Readable	bit	W = Writable k	oit
-n = Value at F	POR	'1' = Bit is se	t	'0' = Bit is cleared x = Bit is unknown			
U = Unimplem	ented bit, read	as '0'					
bit 15-13	Unimplomor	nted: Read as	' <b>O'</b>				
bit 12	-		ultiplier Mode :	Salact hit			
	•	•	•	tiply operations			
	-		for DSP multip				
bit 11			ation Control b				
	0 = No effect	•	loop at end o	f current iteratio	11		
bit 10-8	111 = D0 loo 110 = D0 loo 110 = D0 loo 110 = D0 loo 011 = D0 loo 010 = D0 loo 001 = D0 loo	ping is nested ping is nested ping is nested ping is nested ping is nested ping is nested ping is nested	at 6 levels at 5 levels at 4 levels at 3 levels at 2 levels but not nested				
bit 7	1 = Accumula	A Saturation E ator A saturati ator A saturati	on enabled				
bit 6	1 = Accumula	3 Saturation E ator B saturati ator B saturati	on enabled				
bit 5	1 = Data spa	a Space Write ce write satura ce write satura	ation enabled	gine Saturation	Enable bit		
bit 4	1 = 9.31 satu	cumulator Sat Iration (Super Iration (Norma	,	Select bit			
bit 3	1 = CPU Inte	rrupt Priority L		<b>1, 5)</b> eater (trap exce ss (no trap exce			
bit 2	1 = Program	space visible	ility in Data Spa in data space ble in data spa				
Note 1: Thi	s bit will always	s read '0'.					
	<2:1> are read-						
		-	esting are hand	lled by hardwar	e.		
<b>4</b> ∙ Thi	s hit may he re	ad or cleared	hut not set				

- 4: This bit may be read or cleared, but not set.
- 5: This bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

#### Register 2-6: CORCON: Core Control Register (dsPIC30F and dsPIC33F Devices) (Continued)

- bit 1
   RND: Rounding Mode Select bit

   1 = Biased (conventional) rounding enabled
   0 = Unbiased (convergent) rounding enabled

   bit 0
   IF: Integer or Fractional Multiplier Mode Select bit

   1 = Integer mode enabled for DSP multiply operations
   0 = Fractional mode enabled for DSP multiply operations
- **Note 1:** This bit will always read '0'.
  - **2:** DL<2:1> are read-only.
  - **3:** The first two levels of D0 loop nesting are handled by hardware.
  - 4: This bit may be read or cleared, but not set.
  - 5: This bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0			
VAR	—	US<	<1:0>	EDT <sup>(1)</sup>		DL<2:0>				
bit 15							bit			
5.4.4.6	5.44.0	<b>-</b>	<b>-</b>	<b></b>						
R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0			
SATA bit 7	SATB	SATDW	ACCSAT	IPL3(-,0)	SFA	RND	IF bit			
							Dit			
Legend:										
R = Readable bit		W = Writable bit		U = Unimplemented bit, rea		ad as '0'				
-n = Value at	POR	'1' = Bit is set	t	'0' = Bit is clea	ared	x = Bit is unkr	nown			
bit 15	VAR: Variable	e Exception Pr	ocessing Late	ncy Control bit						
				ption processing						
bit 14	-	ted: Read as '		5	,					
bit 13-12	US<1:0>: DS	P Multiply Uns	igned/Signed	Control bits						
	11 = Reserved									
	10 = DSP engine multiplies are mixed-sign 01 = DSP engine multiplies are unsigned									
		gine multiplies								
bit 11		<b>EDT:</b> Early D0 Loop Termination Control bit <sup>(1)</sup>								
	<ul> <li>1 = Terminate executing D0 loop at end of current loop iteration</li> <li>0 = No effect</li> </ul>									
bit 10-8	<b>DL&lt;2:0&gt;:</b> D0 Loop Nesting Level Status bits 111 = 7 D0 loops active									
	•									
	•									
	•									
	001 = 1 D0 lo 000 = 0 D0 lo	•								
bit 7		Saturation En ator A saturatio								
		ator A saturatio								
bit 6		Saturation En								
	1 = Accumulator B saturation enabled									
bit 5	<ul> <li>0 = Accumulator B saturation disabled</li> <li>SATDW: Data Space Write from DSP Engine Saturation Enable bit</li> </ul>									
	1 = Data space write saturation enabled									
bit 5	0 = Data space write saturation disabled									
bit 5		ACCSAT: Accumulator Saturation Mode Select bit								
bit 4	ACCSAT: Acc			Select bit						
	ACCSAT: Acc 1 = 9.31 satu	ration (super s	aturation)	Select bit						
	ACCSAT: Acc 1 = 9.31 satu 0 = 1.31 satu	ration (super s ration (normal	aturation) saturation)							
bit 4	ACCSAT: Acc 1 = 9.31 satu 0 = 1.31 satu IPL3: CPU In 1 = CPU inter	ration (super s	aturation) saturation) Level Status k vel is greater t	bit 3 <b>(2)</b> han 7						

**Note 1:** This bit always reads as '0'.

- **2:** This bit may be read or cleared, but not set.
- **3:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

Register 2-7:	CORCON: Core Control Register (dsPIC33E Devices) (Continued)
bit 2	<ul> <li>SFA: Stack Frame Active Status bit</li> <li>1 = Stack frame is active. W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values.</li> <li>0 = Stack frame is not active. W14 and W15 address of EDS or Base Data Space</li> </ul>
bit 1	RND: Rounding Mode Select bit
	<ul> <li>1 = Biased (conventional) rounding enabled</li> <li>0 = Unbiased (convergent) rounding enabled</li> </ul>
bit 0	<ul> <li>Integer or Fractional Multiplier Mode Select bit</li> <li>1 = Integer mode enabled for DSP multiply</li> <li>0 = Fractional mode enabled for DSP multiply</li> </ul>

#### **Note 1:** This bit always reads as '0'.

- **2:** This bit may be read or cleared, but not set.
- **3:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.


# **Section 3. Instruction Set Overview**

# HIGHLIGHTS

This section of the manual contains the following major topics:

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3.2	Instruction Set Overview	. 38
3.3	Instruction Set Summary Tables	. 40

# 3.1 INTRODUCTION

The 16-bit MCU and DSC instruction set provides a broad suite of instructions that support traditional microcontroller applications, and a class of instructions that support math intensive applications. Since almost all of the functionality of the 8-bit PIC MCU instruction set has been maintained, this hybrid instruction set allows an easy 16-bit migration path for users already familiar with the PIC microcontroller.

# 3.2 INSTRUCTION SET OVERVIEW

Depending on the device family, the 16-bit MCU and DSC instruction set contains up to 84 instructions, which can be grouped into the functional categories shown in Table 3-1. Table 1-2 defines the symbols used in the instruction summary tables, Table 3-2 through Table 3-11. These tables define the syntax, description, storage and execution requirements for each instruction. Storage requirements are represented in 24-bit instruction words and execution requirements are represented in instruction cycles.

Functional Group	Summary Table	Page Number
Move Instructions	Table 3-2	40
Math Instructions	Table 3-3	41
Logic Instructions	Table 3-4	43
Rotate/Shift Instructions	Table 3-5	44
Bit Instructions	Table 3-6	45
Compare/Skip and Compare/Branch Instructions	Table 3-7	46
Program Flow Instructions	Table 3-8	47
Shadow/Stack Instructions	Table 3-9	49
Control Instructions	Table 3-10	49
DSP Instructions <sup>(1)</sup>	Table 3-11	50

Table 3-1: Instruction Groups

**Note 1:** DSP instructions are only available in the dsPIC30F, dsPIC33F, and dsPIC33E device families.

Most instructions have several different Addressing modes and execution flows, which require different instruction variants. For instance, depending on the device family, there are up to six unique ADD instructions and each instruction variant has its own instruction encoding. Instruction format descriptions and specific instruction operation are provided in **Section 5. "Instruction Descriptions**". Additionally, a composite alphabetized instruction set table is provided in **Section 7. "Reference"**.

## 3.2.1 Multi-Cycle Instructions

As the instruction summary tables show, most instructions execute in a single cycle, with the following exceptions:

- **Note:** The D0 and DIVF instructions are only available in the dsPIC30F, dsPIC33F, and dsPIC33E device families.
- Instructions D0, MOV.D, POP.D, PUSH.D, TBLRDH, TBLRDL, TBLWTH and TBLWTL require 2 cycles to execute
- Instructions DIV.S, DIV.U and DIVF are single-cycle instructions, which should be executed 18 consecutive times as the target of a REPEAT instruction
- Instructions that change the program counter also require 2 cycles to execute, with the
  extra cycle executed as a NOP. Compare-skip instructions, which skip over a 2-word
  instruction, require 3 instruction cycles to execute, with 2 cycles executed as a NOP.
  Compare-branch instructions (dsPIC33E/PIC24E devices only) require 5 instruction cycles
  to execute when the branch is taken.
- The RETFIE, RETLW and RETURN are a special case of an instruction that changes the program counter. These execute in 3 cycles, unless an exception is pending and then they execute in 2 cycles.
  - Note 1: Instructions which access program memory as data, using Program Space Visibility (PSV), will incur a one or two cycle delay for PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices, whereas using PSV in dsPIC33E and PIC24E devices incurs a 4-cycle delay based on Flash memory access time. However, regardless of which device is being used, when the target instruction of a REPEAT loop accesses program memory as data, only the first execution of the target instruction is subject to the delay. See the specific device family reference manual for details.
    - 2: All instructions may incur an additional delay on some device families, depending on Flash memory access time. For example, PIC24E and dsPIC33E devices have a 3-cycle Flash memory access time. However, instruction pipelining increases the effective instruction execution throughput. Refer to Section 2. "CPU" of the specific device family reference manual for details on instruction timing.
    - **3:** All read and read-modify-write operations (including bit operations) on non-CPU Special Function Registers (e.g., I/O Port, peripheral control, or status registers; interrupt flags, etc.) in PIC24E and dsPIC33E devices require 2 instruction cycles to execute. However, all write operations on both CPU and non-CPU Special Function Registers, and all read and read-modify-write operations on CPU Special Function Registers require 1 instruction cycle.

## 3.2.2 Multi-Word Instructions

As defined by Table 3-2, almost all instructions consume one instruction word (24 bits), with the exception of the CALL, D0 and G0T0 instructions, which are Program Flow Instructions, listed in Table 3-8. These instructions require two words of memory because their opcodes embed large literal operands.

# 3.3 INSTRUCTION SET SUMMARY TABLES

### Table 3-2: Move Instructions

As	sembly Syntax	Description	Words	Cycles	Page Number
EXCH	Wns,Wnd	Swap Wns and Wnd	1	1	243
MOV	f {,WREG} <sup>(1)</sup>	Move f to destination	1	1	279
MOV	WREG, f	Move WREG to f	1	1	280
MOV	f,Wnd	Move f to Wnd	1	1(4)	281
MOV	Wns,f	Move Wns to f	1	1	282
MOV.B	#lit8,Wnd	Move 8-bit literal to Wnd	1	1	283
MOV	#lit16,Wnd	Move 16-bit literal to Wnd	1	1	284
MOV	[Ws+Slit10],Wnd	Move [Ws + signed 10-bit offset] to Wnd	1	1(4)	285
MOV	Wns,[Wd+Slit10]	Move Wns to [Wd + signed 10-bit offset]	1	1	286
MOV	Wso,Wdo	Move Wso to Wdo	1	1(4)	287
MOV.D	Ws,Wnd	Move double Ws to Wnd:Wnd + 1	1	2 <sup>(4)</sup>	289
MOV.D	Wns,Wd	Move double Wns:Wns + 1 to Wd	1	2	289
MOVPAG	#lit10,DSRPAG <sup>(2)</sup>	Move 10-bit literal to DSRPAG	1	1	291
MOVPAG	#lit9,DSWPAG <sup>(2)</sup>	Move 9-bit literal to DSWPAG	1	1	291
MOVPAG	#lit8,TBLPAG <sup>(2)</sup>	Move 8-bit literal to TBLPAG	1	1	291
MOVPAG Wr	ı, DSRPAG <sup>(2)</sup>	Move Wn to DSRPAG	1	1	292
MOVPAG Wr	n, DSWPAG <sup>(2)</sup>	Move Wn to DSWPAG	1	1	292
MOVPAG Wr	n, TBLPAG <sup>(2)</sup>	Move Wn to TBLPAG	1	1	292
SWAP	Wn	Wn = byte or nibble swap Wn	1	1	426
TBLRDH	[Ws],Wd	Read high program word to Wd	1	2 <sup>(3)</sup>	427
TBLRDL	[Ws],Wd	Read low program word to Wd	1	2 <sup>(3)</sup>	429
TBLWTH	Ws,[Wd]	Write Ws to high program word	1	2 <sup>(4)</sup>	431
TBLWTL	Ws,[Wd]	Write Ws to low program word	1	2 <sup>(4)</sup>	433

**Note 1:** When the optional {, WREG} operand is specified, the destination of the instruction is WREG. When {, WREG} is not specified, the destination of the instruction is the file register f.

2: The MOVPAG instruction is only available in dsPIC33E and PIC24E devices.

**3:** In dsPIC33E and PIC24E devices, these instructions require 3 additional cycles – compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.

4: In dsPIC33E and PIC24E devices, read and read-modify-write operations on non-CPU Special Function Registers require an additional cycle when compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.

Table 3-3:	Math Instruction			i	i
Ass	embly Syntax	Description	Words	Cycles	Page Number
ADD	f {,WREG} <sup>(1)</sup>	Destination = f + WREG	1	1 <sup>(5)</sup>	99
ADD	#lit10,Wn	Wn = lit10 + Wn	1	1	100
ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	101
ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1 <sup>(5)</sup>	102
ADDC	f {,WREG} <sup>(1)</sup>	Destination = $f + WREG + (C)$	1	1 <sup>(5)</sup>	106
ADDC	#lit10,Wn	Wn = lit10 + Wn + (C)	1	1	107
ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	108
ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1 <sup>(5)</sup>	110
DAW.B	Wn	Wn = decimal adjust Wn	1	1	216
DEC	f {,WREG} <sup>(1)</sup>	Destination = $f - 1$	1	1 <sup>(5)</sup>	217
DEC	Ws,Wd	Wd = Ws - 1	1	1 <sup>(5)</sup>	218
DEC2	f {,WREG} <sup>(1)</sup>	Destination = $f - 2$	1	1 <sup>(5)</sup>	220
DEC2	Ws,Wd	Wd = Ws - 2	1	1 <sup>(5)</sup>	221
DIV.S	Wm, Wn	Signed 16/16-bit integer divide, $Q \rightarrow W0$ , $R \rightarrow W1$	1	18 <b>(2)</b>	224
DIV.SD	Wm, Wn	Signed 32/16-bit integer divide, $Q \rightarrow W0$ , $R \rightarrow W1$	1	18 <sup>(2)</sup>	224
DIV.U	Wm, Wn	Unsigned 16/16-bit integer divide, Q - W0, R $\rightarrow$ W1	1	18 <sup>(2)</sup>	226
DIV.UD	Wm, Wn	Unsigned 32/16-bit integer divide, Q - W0, R $\rightarrow$ W1	1	18 <b>(2)</b>	226
DIVF	Wm, Wn	Signed 16/16-bit fractional divide, Q - W0, R $\rightarrow$ W1	1	18 <sup>(2)</sup>	228
INC	f {,WREG} <sup>(1)</sup>	Destination = f + 1	1	1 <sup>(5)</sup>	254
INC	Ws,Wd	Wd = Ws + 1	1	1 <sup>(5)</sup>	255
INC2	f {,WREG} <sup>(1)</sup>	Destination = f + 2	1	1 <sup>(5)</sup>	257
INC2	Ws,Wd	Wd = Ws + 2	1	1 <sup>(5)</sup>	258
MUL	f	W3:W2 = f * WREG	1	1 <sup>(5)</sup>	303
MUL.SS	Wb,Ws,Wnd	{Wnd + 1,Wnd} = signed(Wb) * signed(Ws)	1	1 <sup>(5)</sup>	305
MUL.SS	Wb,Ws,Acc <sup>(4)</sup>	Accumulator = signed(Wb) * signed(Ws)	1	1 <sup>(5)</sup>	307
MUL.SU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	308
MUL.SU	Wb,Ws,Wnd	{Wnd + 1,Wnd} = signed(Wb) * unsigned(Ws)	1	1 <sup>(5)</sup>	310
MUL.SU	Wb,Ws,Acc <sup>(4)</sup>	Accumulator = signed(Wb) * unsigned(Ws)	1	1 <sup>(5)</sup>	312
MUL.SU	Wb,#lit5,Acc <sup>(4)</sup>	Accumulator = signed(Wb) * unsigned(lit5)	1	1	314
MUL.US	Wb,Ws,Wnd	{Wnd + 1,Wnd} = unsigned(Wb) * signed(Ws)	1	1 <sup>(5)</sup>	315
MUL.US	Wb,Ws,Acc <sup>(4)</sup>	Accumulator = unsigned(Wb) * signed(Ws)	1	1 <sup>(5)</sup>	317
MUL.UU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	319
MUL.UU	Wb,Ws,Wnd	{Wnd + 1,Wnd} = unsigned(Wb) * unsigned(Ws)	1	1 <sup>(5)</sup>	320
MUL.UU	Wb,Ws,Acc <sup>(4)</sup>	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1 <sup>(5)</sup>	322
MUL.UU	Wb,#lit5,Acc <sup>(4)</sup>	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	323
MULW.SS	Wb,Ws,Wnd <sup>(3)</sup>	Wnd = signed(Wb) * signed(Ws)	1	1 <sup>(5)</sup>	324

	Table 3-3:	Math Instructions
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**Note 1:** When the optional {, WREG} operand is specified, the destination of the instruction is WREG. When {, WREG} is not specified, the destination of the instruction is the file register f.

**2:** The divide instructions must be preceded with a "REPEAT #17" instruction, such that they are executed 18 consecutive times.

**3:** These instructions are only available in dsPIC33E and PIC24E devices.

4: These instructions are only available in dsPIC33E devices.

5: In dsPIC33E and PIC24E devices, read and read-modify-write operations on non-CPU Special Function Registers require an additional cycle when compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.

Ass	embly Syntax	Description	Words	Cycles	Page Number
MULW.SU	Wb,Ws,Wnd <sup>(3)</sup>	Wnd = signed(Wb) * unsigned(Ws)	1	1 <sup>(5)</sup>	326
MULW.SU	Wb,#lit5,Wnd <sup>(3)</sup>	Wnd = signed(Wb) * unsigned(lit5)	1	1	328
MULW.US	Wb,Ws,Wnd <sup>(3)</sup>	Wnd = unsigned(Wb) * signed(Ws)	1	1 <sup>(5)</sup>	329
MULW.UU	Wb,Ws,Wnd <sup>(3)</sup>	Wnd = unsigned(Wb) * unsigned(Ws)	1	1 <sup>(5)</sup>	331
MULW.UU	Wb,#lit5,Wnd <sup>(3)</sup>	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	332
SE	Ws,Wnd	Wnd = signed-extended Ws	1	1 <sup>(5)</sup>	393
SUB	f {,WREG} <sup>(1)</sup>	Destination = $f - WREG$	1	1 <sup>(5)</sup>	405
SUB	#lit10,Wn	Wn = Wn - lit10	1	1	406
SUB	Wb,#lit5,Wd	Wd = Wb - lit5	1	1	407
SUB	Wb,Ws,Wd	Wd = Wb - Ws	1	1 <sup>(5)</sup>	408
SUBB	f {,WREG} <sup>(1)</sup>	Destination = $f - WREG - (\overline{C})$	1	1 <sup>(5)</sup>	411
SUBB	#lit10,Wn	$Wn = Wn - lit10 - (\overline{C})$	1	1	412
SUBB	Wb,#lit5,Wd	$Wd = Wb - lit5 - (\overline{C})$	1	1	413
SUBB	Wb,Ws,Wd	$Wd = Wb - Ws - (\overline{C})$	1	1 <sup>(5)</sup>	415
SUBBR	f {,WREG} <sup>(1)</sup>	Destination = WREG – f – ( $\overline{C}$ )	1	1 <sup>(5)</sup>	417
SUBBR	Wb,#lit5,Wd	$Wd = lit5 - Wb - (\overline{C})$	1	1	418
SUBBR	Wb,Ws,Wd	$Wd = Ws - Wb - (\overline{C})$	1	1 <sup>(5)</sup>	420
SUBR	f {,WREG} <sup>(1)</sup>	Destination = WREG – f	1	1 <sup>(5)</sup>	422
SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	423
SUBR	Wb,Ws,Wd	Wd = Ws - Wb	1	1 <sup>(5)</sup>	424
ZE	Ws,Wnd	Wnd = zero-extended Ws	1	1 <sup>(5)</sup>	442

### Table 3-3: Math Instructions (Continued)

**Note 1:** When the optional {, WREG} operand is specified, the destination of the instruction is WREG. When {, WREG} is not specified, the destination of the instruction is the file register f.

**2:** The divide instructions must be preceded with a "REPEAT #17" instruction, such that they are executed 18 consecutive times.

- **3:** These instructions are only available in dsPIC33E and PIC24E devices.
- 4: These instructions are only available in dsPIC33E devices.
- 5: In dsPIC33E and PIC24E devices, read and read-modify-write operations on non-CPU Special Function Registers require an additional cycle when compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.

	Assembly Syntax	Description	Words	Cycles	Page Number
AND	f {,WREG} <sup>(1)</sup>	Destination = f .AND. WREG	1	1 <sup>(2)</sup>	112
AND	#lit10,Wn	Wn = lit10 .AND. Wn	1	1	113
AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	114
AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1 <sup>(2)</sup>	115
CLR	f	f = 0x0000	1	1	184
CLR	WREG	WREG = 0x0000	1	1	184
CLR	Wd	Wd = 0x0000	1	1	185
COM	f {,WREG} <sup>(1)</sup>	Destination = $\overline{f}$	1	1(2)	189
COM	Ws,Wd	$Wd = \overline{Ws}$	1	1 <sup>(2)</sup>	190
IOR	f {,WREG} <sup>(1)</sup>	Destination = f .IOR. WREG	1	1(2)	260
IOR	#lit10,Wn	Wn = lit10 .IOR. Wn	1	1	261
IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	262
IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1(2)	263
NEG	f {,WREG} <sup>(1)</sup>	Destination = $\overline{f}$ + 1	1	1(2)	333
NEG	Ws,Wd	$Wd = \overline{Ws} + 1$	1	1 <sup>(2)</sup>	333
SETM	f	f = 0xFFFF	1	1	395
SETM	WREG	WREG = 0xFFFF	1	1	395
SETM	Wd	Wd = 0xFFFF	1	1	396
XOR	f {,WREG} <sup>(1)</sup>	Destination = f .XOR. WREG	1	1(2)	437
XOR	#lit10,Wn	Wn = lit10 .XOR. Wn	1	1	438
XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	439
XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1(2)	440

Note 1: When the optional {, WREG} operand is specified, the destination of the instruction is WREG. When  $\{, WREG\}$  is not specified, the destination of the instruction is the file register f.

2: In dsPIC33E and PIC24E devices, read and read-modify-write operations on non-CPU Special Function Registers require an additional cycle when compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.

	Assembly Syntax	Description	Words	Cycles	Page Number
ASR	f {,WREG} <sup>(1)</sup>	Destination = arithmetic right shift f, LSb $\rightarrow$ C	1	1 <sup>(2)</sup>	117
ASR	Ws,Wd	Wd = arithmetic right shift Ws, LSb $\rightarrow$ C	1	1(2)	119
ASR	Wb,#lit4,Wnd	Wnd = arithmetic right shift Wb by lit4, LSb $\rightarrow$ C	1	1	121
ASR	Wb,Wns,Wnd	Wnd = arithmetic right shift Wb by Wns, LSb $\rightarrow$ C	1	1	122
LSR	f {,WREG} <sup>(1)</sup>	Destination = logical right shift f, LSb $\rightarrow$ C	1	1 <sup>(2)</sup>	269
LSR	Ws,Wd	Wd = logical right shift Ws, LSb $\rightarrow$ C	1	1(2)	271
LSR	Wb,#lit4,Wnd	Wnd = logical right shift Wb by lit4, LSb $\rightarrow$ C	1	1	273
LSR	Wb,Wns,Wnd	Wnd = logical right shift Wb by Wns, LSb $\rightarrow$ C	1	1	274
RLC	f {,WREG} <sup>(1)</sup>	Destination = rotate left through Carry f	1	1(2)	373
RLC	Ws,Wd	Wd = rotate left through Carry Ws	1	1(2)	375
RLNC	f {,WREG} <sup>(1)</sup>	Destination = rotate left (no Carry) f	1	1(2)	377
RLNC	Ws,Wd	Wd = rotate left (no Carry) Ws	1	1(2)	379
RRC	f {,WREG} <sup>(1)</sup>	Destination = rotate right through Carry f	1	1(2)	381
RRC	Ws,Wd	Wd = rotate right through Carry Ws	1	1(2)	383
RRNC	f {,WREG} <sup>(1)</sup>	Destination = rotate right (no Carry) f	1	1(2)	385
RRNC	Ws,Wd	Wd = rotate right (no Carry) Ws	1	1(2)	387
SL	f {,WREG} <sup>(1)</sup>	Destination = left shift f, MSb $\rightarrow$ C	1	1(2)	399
SL	Ws,Wd	Wd = left shift Ws, MSb $\rightarrow$ C	1	1(2)	401
SL	Wb,#lit4,Wnd	Wnd = left shift Wb by lit4, MSb $\rightarrow$ C	1	1	403
SL	Wb,Wns,Wnd	Wnd = left shift Wb by Wns, MSb $\rightarrow$ C	1	1	404

## Table 3-5: Rotate/Shift Instructions

**Note 1:** When the optional {, WREG} operand is specified, the destination of the instruction is WREG. When {, WREG} is not specified, the destination of the instruction is the file register f.

2: In dsPIC33E and PIC24E devices, read and read-modify-write operations on non-CPU Special Function Registers require an additional cycle when compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.

Table 3-6:	Bit Instructions				
Asse	embly Syntax	Description	Words	Cycles <sup>(1)</sup>	Page Number
BCLR	f,#bit4	Bit clear f	1	1	123
BCLR	Ws,#bit4	Bit clear Ws	1	1	124
BSET	f,#bit4	Bit set f	1	1	152
BSET	Ws,#bit4	Bit set Ws	1	1	153
BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	155
BSW.Z	Ws,Wb	Write Z bit to Ws <wb></wb>	1	1	155
BTG	f,#bit4	Bit toggle f	1	1	157
BTG	Ws,#bit4	Bit toggle Ws	1	1	158
BTST	f,#bit4	Bit test f to Z	1	1	168
BTST.C	Ws,#bit4	Bit test Ws to C	1	1	169
BTST.Z	Ws,#bit4	Bit test Ws to Z	1	1	169
BTST.C	Ws,Wb	Bit test Ws <wb> to C</wb>	1	1	171
BTST.Z	Ws,Wb	Bit test Ws <wb> to Z</wb>	1	1	171
BTSTS	f,#bit4	Bit test f to Z, then set f	1	1	173
BTSTS.C	Ws,#bit4	Bit test Ws to C then set Ws	1	1	175
BTSTS.Z	Ws,#bit4	Bit test Ws to Z then set Ws	1	1	175
FBCL	Ws,Wnd	Find bit change from left (MSb) side	1	1	244
FF1L	Ws,Wnd	Find first one from left (MSb) side	1	1	246
FF1R	Ws,Wnd	Find first one from right (LSb) side	1	1	248
1 1 <b>T</b> V				<u> </u>	

Table 3-6: Bit Instructions

**Note 1:** In dsPIC33E and PIC24E devices, read and read-modify-write operations on non-CPU Special Function Registers require an additional cycle when compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.

Asse	embly Syntax	Description	Words	Cycles <sup>(1)</sup>	Page Number
BTSC	f,#bit4	Bit test f, skip if clear	1	1 (2 or 3) <sup>(5)</sup>	160
BTSC	Ws,#bit4	Bit test Ws, skip if clear	1	1 (2 or 3) <sup>(5)</sup>	162
BTSS	f,#bit4	Bit test f, skip if set	1	1 (2 or 3) <sup>(5)</sup>	164
BTSS	Ws,#bit4	Bit test Ws, skip if set	1	1 (2 or 3) <sup>(5)</sup>	166
СР	f	Compare (f – WREG)	1	1 <sup>(5)</sup>	191
СР	Wb,#lit5 <sup>(2)</sup>	Compare (Wb – lit5)	1	1	192
СР	Wb,#lit8 <sup>(3)</sup>	Compare (Wb – lit8)	1	1	193
СР	Wb,Ws	Compare (Wb – Ws)	1	1 <sup>(5)</sup>	194
CP0	f	Compare (f – 0x0000)	1	1 <sup>(5)</sup>	196
CP0	Ws	Compare (Ws – 0x0000)	1	1 <sup>(5)</sup>	197
СРВ	f	Compare with Borrow (f – WREG – $\overline{C}$ )	1	1 <sup>(5)</sup>	198
СРВ	Wb,#lit5 <sup>(2)</sup>	Compare with Borrow (Wb – lit5 – $\overline{C}$ )	1	1	199
СРВ	Wb,#lit8 <sup>(3)</sup>	Compare with Borrow (Wb – lit8 – $\overline{C}$ )	1	1	200
СРВ	Wb,Ws	Compare with Borrow (Wb – Ws – $\overline{C}$ )	1	1 <sup>(5)</sup>	201
CPBEQ	Wb,Wn,Expr <sup>(3)</sup>	Compare Wb with Wn, branch if =	1	1 (5) <sup>(4)</sup>	203
CPBGT	Wb,Wn,Expr <sup>(3)</sup>	Signed compare Wb with Wn, branch if >	1	1 (5) <sup>(4)</sup>	204
CPBLT	Wb,Wn,Expr <sup>(3)</sup>	Signed compare Wb with Wn, branch if <	1	1 (5) <sup>(4)</sup>	205
CPBNE	Wb,Wn,Expr <sup>(3)</sup>	Compare Wb with Wn, branch if ≠	1	1 (5) <sup>(4)</sup>	204
CPSEQ	Wb, Wn	Compare (Wb – Wn), skip if =	1	1 (2 or 3)	207
CPSGT	Wb, Wn	Signed compare (Wb – Wn), skip if >	1	1 (2 or 3)	211
CPSLT	Wb, Wn	Signed compare (Wb – Wn), skip if <	1	1 (2 or 3)	212
CPSNE	Wb, Wn	Compare (Wb – Wn), skip if ≠	1	1 (2 or 3)	214

### Table 3-7: Compare/Skip and Compare/Branch Instructions

**Note 1:** Conditional skip instructions execute in 1 cycle if the skip is not taken, 2 cycles if the skip is taken over a one-word instruction and 3 cycles if the skip is taken over a two-word instruction.

2: This instruction is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices.

3: This instruction is only available in dsPIC33E and PIC24E devices.

4: Compare-branch instructions in dsPIC33E/PIC24E devices execute in 1 cycle if the branch is not taken and 5 cycles if the branch is taken.

5: In dsPIC33E and PIC24E devices, read and read-modify-write operations on non-CPU Special Function Registers require an additional cycle when compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.

Ass	embly Syntax	Description	Words	Cycles	Page Number
BRA	Expr	Branch unconditionally	1	2 <sup>(8)</sup>	126
BRA	Wn	Computed branch	1	2 <sup>(8)</sup>	128
BRA	C,Expr	Branch if Carry (no Borrow)	1	1 (2) <sup>(1,8)</sup>	130
BRA	GE,Expr	Branch if greater than or equal	1	1 (2) <sup>(1,8)</sup>	132
BRA	GEU,Expr	Branch if unsigned greater than or equal	1	1 (2) <sup>(1,8)</sup>	134
BRA	GT,Expr	Branch if greater than	1	1 (2) <sup>(1,8)</sup>	135
BRA	GTU,Expr	Branch if unsigned greater than	1	1 (2) <sup>(1,8)</sup>	136
BRA	LE,Expr	Branch if less than or equal	1	1 (2) <sup>(1,8)</sup>	137
BRA	LEU,Expr	Branch if unsigned less than or equal	1	1 (2) <sup>(1,8)</sup>	138
BRA	LT, Expr	Branch if less than	1	1 (2) <sup>(1,8)</sup>	139
BRA	LTU,Expr	Branch if unsigned less than	1	1 (2) <sup>(1,8)</sup>	140
BRA	N,Expr	Branch if Negative	1	1 (2) <sup>(1,8)</sup>	141
BRA	NC,Expr	Branch if not Carry (Borrow)	1	1 (2) <sup>(1,8)</sup>	142
BRA	NN,Expr	Branch if not Negative	1	1 (2) <sup>(1,8)</sup>	143
BRA	NOV,Expr	Branch if not Overflow	1	1 (2) <sup>(1,8)</sup>	144
BRA	NZ,Expr	Branch if not Zero	1	1 (2) <sup>(1,8)</sup>	145
BRA	0A,Expr	Branch if Accumulator A Overflow	1	1 (2) <sup>(1,8)</sup>	146
BRA	OB,Expr	Branch if Accumulator B Overflow	1	1 (2) <sup>(1,8)</sup>	147
BRA	0V,Expr	Branch if Overflow	1	1 (2) <sup>(1,8)</sup>	148
BRA	SA, Expr	Branch if Accumulator A Saturate	1	1 (2) <sup>(1,8)</sup>	149
BRA	SB, Expr	Branch if Accumulator B Saturate	1	1 (2) <sup>(1,8)</sup>	150
BRA	Z,Expr	Branch if Zero	1	1 (2) <sup>(1,8)</sup>	151
CALL	Expr	Call subroutine	2	2 <sup>(8)</sup>	177
CALL	Wn	Call indirect subroutine	1	2 <sup>(8)</sup>	180
CALL.L	Wn <sup>(4)</sup>	Call indirect subroutine (long address)	1	4	183
DO	<pre>#lit14,Expr(6)</pre>	Do code through PC + Expr, (lit14 + 1) times	2	2	230
D0	<pre>#lit15,Expr<sup>(7)</sup></pre>	Do code through PC + Expr, (lit15 + 1) times	2	2	233
DO	Wn,Expr <sup>(3)</sup>	Do code through PC + Expr, (Wn + 1) times	2	2	235
GOTO	Expr	Go to address	2	2 <sup>(8)</sup>	250
GOTO	Wn	Go to address indirectly	1	2 <sup>(8)</sup>	251
GOTO.L	Wn <sup>(4)</sup>	Go to indirect (long address)	1	4	253
RCALL	Expr	Relative call	1	2 <sup>(8)</sup>	347
RCALL	Wn	Computed call	1	2 <sup>(8)</sup>	351
REPEAT	#lit14 <sup>(5)</sup>	Repeat next instruction (lit14 + 1) times	1	1	355

Table 3-8: Program Flow Instructions

**Note 1:** Conditional branch instructions execute in 1 cycle if the branch is not taken, or 2 cycles if the branch is taken.

- **2:** RETURN instructions execute in 3 cycles, but if an exception is pending, they execute in 2 cycles.
- 3: This instruction is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.
- 4: This instruction is only available in dsPIC33E and PIC24E devices.
- 5: This instruction is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices.
- 6: This instruction is only available in dsPIC30F and dsPIC33F devices.
- 7: This instruction is only available in dsPIC33E devices.
- 8: In dsPIC33E and PIC24E devices, these instructions require 2 additional cycles (4 cycles overall) when the branch is taken.
- 9: In dsPIC33E and PIC24E devices, these instructions require 3 additional cycles.

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Assembly Syntax	Description	Words	Cycles	Page Number
REPEAT #lit15 <sup>(4)</sup>	Repeat next instruction (lit15 + 1) times	1	1	357
REPEAT Wn	Repeat next instruction (Wn + 1) times	1	1	359
RETFIE	Return from interrupt enable		3 (2) <sup>(2,9)</sup>	365
RETLW #lit10,Wn	#lit10,Wn Return with lit10 in Wn 1 3 (2) <sup>(2,9)</sup>		367	
RETURN	Return from subroutine	1	3 (2) <sup>(2,9)</sup>	371

### Table 3-8: Program Flow Instructions (Continued)

**Note 1:** Conditional branch instructions execute in 1 cycle if the branch is not taken, or 2 cycles if the branch is taken.

2: RETURN instructions execute in 3 cycles, but if an exception is pending, they execute in 2 cycles.

3: This instruction is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.

4: This instruction is only available in dsPIC33E and PIC24E devices.

5: This instruction is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices.

6: This instruction is only available in dsPIC30F and dsPIC33F devices.

7: This instruction is only available in dsPIC33E devices.

8: In dsPIC33E and PIC24E devices, these instructions require 2 additional cycles (4 cycles overall) when the branch is taken.

9: In dsPIC33E and PIC24E devices, these instructions require 3 additional cycles.

Assei	mbly Syntax	Description	Words	Cycles	Page Number
LNK	#lit14	Link Frame Pointer	1	1	267
POP	f	POP TOS to f	1	1	337
POP	Wdo	POP TOS to Wdo	1	1	338
POP.D	Wnd	Double POP from TOS to Wnd:Wnd + 1	1	2	339
POP.S		POP shadow registers	1	1	340
PUSH	f	PUSH f to TOS	1	1(1)	341
PUSH	Wso	PUSH Wso to TOS	1	1(1)	342
PUSH.D	Wns	PUSH double Wns:Wns + 1 to TOS	1	2	343
PUSH.S		PUSH shadow registers	1	1	345
ULNK		Unlink Frame Pointer	1	1	435

#### Table 3-9:Shadow/Stack Instructions

**Note 1:** In dsPIC33E and PIC24E devices, read and read-modify-write operations on non-CPU Special Function Registers require an additional cycle when compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.

### Table 3-10: Control Instructions

Assemi	oly Syntax	Description	Words	Cycles	Page Number
CLRWDT		Clear Watchdog Timer	1	1	188
DISI	#lit14	Disable interrupts for (lit14 + 1) instruction cycles	1	1	223
NOP		No operation	1	1	336
NOPR		No operation	1	1	336
PWRSAV	#lit1	Enter Power-saving mode lit1	1	1	346
RESET		Software device Reset	1	1	363

	Assembly Syntax	Description	Words	Cycles	Page Number
ADD	Acc	Add accumulators	1	1	103
ADD	Wso,#Slit4,Acc	16-bit signed add to Acc	1	1(1)	104
CLR	Acc,[Wx],Wxd,[Wy],Wyd,AWB	Clear Acc	1	1	186
ED	Wm*Wm,Acc,[Wx],[Wy],Wxd	Euclidean distance (no accumulate)	1	1	239
EDAC	Wm*Wm,Acc,[Wx],[Wy],Wxd	Euclidean distance	1	1	241
LAC	Wso,#Slit4,Acc	Load Acc	1	1(1)	265
MAC	Wm*Wn,Acc,[Wx],Wxd,[Wy],Wyd,AWB	Multiply and accumulate	1	1	275
MAC	Wm*Wm,Acc,[Wx],Wxd,[Wy],Wyd	Square and accumulate	1	1	277
MOVSAC	Acc,[Wx],Wxd,[Wy],Wyd,AWB	Move Wx to Wxd and Wy to Wyd	1	1	293
MPY	Wm*Wn,Acc,[Wx],Wxd,[Wy],Wyd	Multiply Wn by Wm to Acc	1	1	295
MPY	Wm*Wm,Acc,[Wx],Wxd,[Wy],Wyd	Square to Acc	1	1	297
MPY.N	Wm*Wn,Acc,[Wx],Wxd,[Wy],Wyd	-(Multiply Wn by Wm) to Acc	1	1	299
MSC	Wm*Wn,Acc,[Wx],Wxd,[Wy],Wyd,AWB	Multiply and subtract from Acc	1	1	301
NEG	Acc	Negate Acc	1	1	335
SAC	Acc,#Slit4,Wdo	Store Acc	1	1	389
SAC.R	Acc,#Slit4,Wdo	Store rounded Acc	1	1	391
SFTAC	Acc,#Slit6	Arithmetic shift Acc by Slit6	1	1	397
SFTAC	Acc,Wn	Arithmetic shift Acc by (Wn)	1	1	398
SUB	Acc	Subtract accumulators	1	1	410

### Table 3-11: DSP Instructions (dsPIC30F, dsPIC33F and dsPIC33E Devices)

**Note 1:** In dsPIC33E and PIC24E devices, read and read-modify-write operations on non-CPU Special Function Registers require an additional cycle when compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.



# **Section 4. Instruction Set Details**

# HIGHLIGHTS

This section of the manual contains the following major topics:

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4

Instruction Set Details

# 4.1 DATA ADDRESSING MODES

The 16-bit MCU and DSC devices support three native Addressing modes for accessing data memory, along with several forms of immediate addressing. Data accesses may be performed using file register addressing, register direct or indirect addressing, and immediate addressing, allow a fixed value to be used by the instruction.

File register addressing provides the ability to operate on data stored in the lower 8K of data memory (Near RAM), and also move data between the working registers and the entire 64K data space. Register direct addressing is used to access the 16 memory mapped working registers, W0:W15. Register indirect addressing is used to efficiently operate on data stored in the entire 64K data space (and also Extended Data Space, in the case of dsPIC33E/PIC24E), using the contents of the working registers as an effective address. Immediate addressing does not access data memory, but provides the ability to use a constant value as an instruction operand. The address range of each mode is summarized in Table 4-1.

Addressing Mode	Address Range
File Register	0x0000-0x1FFF <sup>(1)</sup>
Register Direct	0x0000-0x001F (working register array W0:W15)
Register Indirect	0x0000-0xFFFF
Immediate	N/A (constant value)

Table 4-1: 16-bit MCU and DSC Addressing Modes

**Note 1:** The address range for the File Register MOV is 0x0000-0xFFFE.

### 4.1.1 File Register Addressing

File register addressing is used by instructions which use a predetermined data address as an operand for the instruction. The majority of instructions that support file register addressing provide access to the lower 8 Kbytes of data memory, which is called the Near RAM. However, the MOV instruction provides access to all 64 Kbytes of memory using file register addressing. This allows the loading of the data from any location in data memory to any working register, and storing the contents of any working register to any location in data memory. It should be noted that file register addressing supports both byte and word accesses of data memory, with the exception of the MOV instruction, which accesses all 64K of memory as words. Examples of file register addressing are shown in Example 4-1.

Most instructions, which support file register addressing, perform an operation on the specified file register and the default working register WREG (see **Section 2.4 "Default Working Register (WREG)**"). If only one operand is supplied in the instruction, WREG is an implied operand and the operation results are stored back to the file register. In these cases, the instruction is effectively a read-modify-write instruction. However, when both the file register and the WREG register are specified in the instruction, the operation results are stored in the WREG register are stored in the instruction, the operation results are stored in the WREG register and the contents of the file register are unchanged. Sample instructions that show the interaction between the file register and the WREG register are shown in Example 4-2.

**Note:** Instructions which support file register addressing use 'f' as an operand in the instruction summary tables of **Section 3. "Instruction Set Overview**".

Example 4-1: File Register Addressing

```
DEC
             0x1000
                               : decrement data stored at 0x1000
Before Instruction:
    Data Memory 0x1000 = 0x5555
After Instruction:
    Data Memory 0 \times 1000 = 0 \times 5554
    MOV
             0x27FE, W0
                              ; move data stored at 0x27FE to W0
Before Instruction:
    W0 = 0 \times 5555
    Data Memory 0x27FE = 0x1234
After Instruction:
    W0 = 0 \times 1234
    Data Memory 0x27FE = 0x1234
```

```
Example 4-2: File Register Addressing and WREG
```

```
AND
              0×1000
                                  ; AND 0x1000 with WREG, store to 0x1000
Before Instruction:
    W0 (WREG) = 0 \times 332C
    Data Memory 0 \times 1000 = 0 \times 5555
After Instruction:
    W0 (WREG) = 0 \times 332C
    Data Memory 0 \times 1000 = 0 \times 1104
    AND
                                 ; AND 0x1000 with WREG, store to WREG
              0x1000, WREG
Before Instruction:
    W0 (WREG) = 0 \times 332C
    Data Memory 0 \times 1000 = 0 \times 5555
After Instruction:
    WO (WREG) = 0 \times 1104
    Data Memory 0 \times 1000 = 0 \times 5555
```

## 4.1.2 Register Direct Addressing

Register direct addressing is used to access the contents of the 16 working registers (W0:W15). The Register Direct Addressing mode is fully orthogonal, which allows any working register to be specified for any instruction that uses register direct addressing, and it supports both byte and word accesses. Instructions which employ register direct addressing use the contents of the specified working register as data to execute the instruction, therefore this Addressing mode is useful only when data already resides in the working register core. Sample instructions which utilize register direct addressing are shown in Example 4-3.

Another feature of register direct addressing is that it provides the ability for dynamic flow control. Since variants of the D0 and REPEAT instruction support register direct addressing, flexible looping constructs may be generated using these instructions.

Note: Instructions which must use register direct addressing, use the symbols Wb, Wn, Wns and Wnd in the summary tables of **Section 3. "Instruction Set Overview**". Commonly, register direct addressing may also be used when register indirect addressing may be used. Instructions which use register indirect addressing, use the symbols Wd and Ws in the summary tables of **Section 3. "Instruction Set Overview**". Instruction Set

Deta

S

EXCH W2, W3	; Exchange W2 and W3
Before Instruction:	
W2 = 0×3499 W3 = 0×003D	
After Instruction:	
W2 = 0×003D W3 = 0×3499	
IOR #0×44, W0	; Inclusive-OR 0x44 and W0
Before Instruction:	
$W0 = 0 \times 9C2E$	
After Instruction:	
W0 = 0×9C6E	
SL W6, W7, W8	; Shift left W6 by W7, and store to W8
Before Instruction:	
$W6 = 0 \times 000C$	
$W7 = 0 \times 0008$ $W8 = 0 \times 1234$	
After Instruction:	
$W6 = 0 \times 000C$	
$W7 = 0 \times 0008$ $W8 = 0 \times 0000$	
WG - 0X0000	

### Example 4-3: Register Direct Addressing

### 4.1.3 Register Indirect Addressing

Register indirect addressing is used to access any location in data memory by treating the contents of a working register as an Effective Address (EA) to data memory. Essentially, the contents of the working register become a pointer to the location in data memory which is to be accessed by the instruction.

This Addressing mode is powerful, because it also allows one to modify the contents of the working register, either before or after the data access is made, by incrementing or decrementing the EA. By modifying the EA in the same cycle that an operation is being performed, register indirect addressing allows for the efficient processing of data that is stored sequentially in memory. The modes of indirect addressing supported by the 16-bit MCU and DSC devices are shown in Table 4-2.

Indirect Mode	Syntax	Function (Byte Instruction)	Function (Word Instruction)	Description
No Modification	[Wn]	EA = [Wn]	EA = [Wn]	The contents of Wn forms the EA.
Pre-Increment	[++Wn]	EA = [Wn + = 1]	EA = [Wn + = 2]	Wn is pre-incremented to form the EA.
Pre-Decrement	[Wn]	EA = [Wn - = 1]	EA = [Wn - = 2]	Wn is pre-decremented to form the EA.
Post-Increment	[Wn++]	EA = [Wn]+ = 1	EA = [Wn]+ = 2	The contents of Wn forms the EA, then Wn is post-incremented.
Post-Decrement	[Wn]	EA = [Wn] - = 1	EA = [Wn] - = 2	The contents of Wn forms the EA, then Wn is post-decremented.
Register Offset	[Wn+Wb]	EA = [Wn + Wb]	EA = [Wn + Wb]	The sum of Wn and Wb forms the EA. Wn and Wb are not modified.

Table 4-2: Indirect Addressing Modes

Table 4-2 shows that four Addressing modes modify the EA used in the instruction, and this allows the following updates to be made to the working register: post-increment, post-decrement, pre-increment and pre-decrement. Since all EAs must be given as byte addresses, support is provided for Word mode instructions by scaling the EA update by 2. Namely, in Word mode, pre/post-decrements subtract 2 from the EA stored in the working register, and pre/post-increments add 2 to the EA. This feature ensures that after an EA modification is made, the EA will point to the next adjacent word in memory. Example 4-4 shows how indirect addressing may be used to update the EA.

Table 4-2 also shows that the Register Offset mode addresses data which is offset from a base EA stored in a working register. This mode uses the contents of a second working register to form the EA by adding the two specified working registers. This mode does not scale for Word mode instructions, but offers the complete offset range of 64 Kbytes. Note that neither of the working registers used to form the EA are modified. Example 4-5 shows how register offset indirect addressing may be used to access data memory.

**Note:** The MOV with offset instructions (see pages 285 and 286) provides a literal addressing offset ability to be used with indirect addressing. In these instructions, the EA is formed by adding the contents of a working register to a signed 10-bit literal. Example 4-6 shows how these instructions may be used to move data to and from the working register array.

#### Example 4-4: Indirect Addressing with Effective Address Update

MOV.B [W0++], [W13]	; byte move [W0] to [W13] ; post-inc W0, post-dec W13
Before Instruction:	
W0 = 0x2300 W13 = 0x2708 Data Memory 0x2300 = 0x7783 Data Memory 0x2708 = 0x904E	
After Instruction:	
W0 = 0x2301 W13 = 0x2707 Data Memory 0x2300 = 0x7783 Data Memory 0x2708 = 0x9083	
ADD W1, [W5], [++W8]	; pre-dec W5, pre-inc W8 ; add W1 to [W5], store in [W8]
Before Instruction:	
W1 = 0x0800 W5 = 0x2200 W8 = 0x2400 Data Memory 0x21FE = 0x7783 Data Memory 0x2402 = 0xAACC	
After Instruction:	
W1 = 0x0800 W5 = 0x21FE W8 = 0x2402 Data Memory 0x21FE = 0x7783 Data Memory 0x2402 = 0x7F83	

```
MOV.B [W0+W1], [W7++] ; byte move [W0+W1] to W7, post-inc W7
Before Instruction:
    W0 = 0 \times 2300
    W1 = 0 \times 01 FE
    W7 = 0 \times 1000
    Data Memory 0x24FE = 0x7783
    Data Memory 0x1000 = 0x11DC
After Instruction:
    W0 = 0 \times 2300
    W1 = 0×01FE
   W7 = 0 \times 1001
   Data Memory 0x24FE = 0x7783
    Data Memory 0 \times 1000 = 0 \times 1183
                               ; load ACCA with [W0+W8]
             [W0+W8], A
    LAC
                                       ; (sign-extend and zero-backfill)
Before Instruction:
    W0 = 0 \times 2344
    W8 = 0 \times 0008
    ACCA = 0 \times 00 7877 9321
    Data Memory 0x234C = 0xE290
After Instruction:
    W0 = 0 \times 2344
    W8 = 0 \times 0008
    ACCA = 0×FF E290 0000
    Data Memory 0x234C = 0xE290
```

```
Example 4-6: Move with Literal Offset Instructions
```

```
MOV
             [W0+0x20], W1
                                     ; move [W0+0x20] to W1
Before Instruction:
    W0 = 0 \times 1200
    W1 = 0x01FE
    Data Memory 0x1220 = 0xFD27
After Instruction:
    W0 = 0 \times 1200
    W1 = 0 \times FD27
    Data Memory 0x1220 = 0xFD27
    MOV
            W4, [W8-0x300]
                               ; move W4 to [W8-0x300]
Before Instruction:
    W4 = 0 \times 3411
    W8 = 0 \times 2944
    Data Memory 0x2644 = 0xCB98
After Instruction:
    W4 = 0 \times 3411
    W8 = 0 \times 2944
    Data Memory 0x2644 = 0x3411
```

### 4.1.3.1 REGISTER INDIRECT ADDRESSING AND THE INSTRUCTION SET

The Addressing modes presented in Table 4-2 demonstrate the Indirect Addressing mode capability of the 16-bit MCU and DSC devices. Due to operation encoding and functional considerations, not every instruction which supports indirect addressing supports all modes shown in Table 4-2. The majority of instructions which use indirect addressing support the No Modify, Pre-Increment, Pre-Decrement, Post-Increment and Post-Decrement Addressing modes. The MOV instructions, and several accumulator-based DSP instructions (dsPIC30F, dsPIC33F, and dsPIC33E devices only), are also capable of using the Register Offset Addressing mode.

Note: Instructions which use register indirect addressing use the operand symbols Wd and Ws in the summary tables of Section 3. "Instruction Set Overview".

# 4.1.3.2 DSP MAC INDIRECT ADDRESSING MODES (dsPIC30F, dsPIC33F, AND dsPIC33E DEVICES)

A special class of Indirect Addressing modes is utilized by the DSP MAC instructions. As is described later in **Section 4.14 "DSP MAC Instructions (dsPIC30F, dsPIC33F and dsPIC33E Devices)**", the DSP MAC class of instructions are capable of performing two fetches from memory using effective addressing. Since DSP algorithms frequently demand a broader range of address updates, the Addressing modes offered by the DSP MAC instructions provide greater range in the size of the effective address update which may be made. Table 4-3 shows that both X and Y prefetches support Post-Increment and Post-Decrement Addressing modes, with updates of 2, 4 and 6 bytes. Since DSP instructions only execute in Word mode, no provisions are made for odd sized EA updates.

Addressing Mode	X Memory	Y Memory
Indirect with no modification	EA = [Wx]	EA = [Wy]
Indirect with Post-Increment by 2	EA = [Wx] + = 2	EA = [Wy] + = 2
Indirect with Post-Increment by 4	EA = [Wx] + = 4	EA = [Wy] + = 4
Indirect with Post-Increment by 6	EA = [Wx] + = 6	EA = [Wy] + = 6
Indirect with Post-Decrement by 2	EA = [Wx] – = 2	EA = [Wy] – = 2
Indirect with Post-Decrement by 4	EA = [Wx] - = 4	EA = [Wy] – = 4
Indirect with Post-Decrement by 6	EA = [Wx] - = 6	EA = [Wy] – = 6
Indirect with Register Offset	EA = [W9 + W12]	EA = [W11 + W12]

Table 4-3: DSP MAC Indirect Addressing Modes

Note: As described in Section 4.14 "DSP MAC Instructions (dsPIC30F, dsPIC33F and dsPIC33E Devices)", only W8 and W9 may be used to access X Memory, and only W10 and W11 may be used to access Y Memory.

# 4.1.3.3 MODULO AND BIT-REVERSED ADDRESSING MODES (dsPIC30F, dsPIC33F, AND dsPIC33E DEVICES)

The 16-bit DSC architecture provides support for two special Register Indirect Addressing modes, which are commonly used to implement DSP algorithms. Modulo (or circular) addressing provides an automated means to support circular data buffers in X and/or Y memory. Modulo buffers remove the need for software to perform address boundary checks, which can improve the performance of certain algorithms. Similarly, bit-reversed addressing allows one to access the elements of a buffer in a nonlinear fashion. This Addressing mode simplifies data re-ordering for radix-2 FFT algorithms and provides a significant reduction in FFT processing time.

Both of these Addressing modes are powerful features of the dsPIC30F, dsPIC33F, and dsPIC33E architectures, which can be exploited by any instruction that uses indirect addressing. Refer to the specific device family reference manual for details on using modulo and bit-reversed addressing.

Instruction Set

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## 4.1.4 Immediate Addressing

In immediate addressing, the instruction encoding contains a predefined constant operand, which is used by the instruction. This Addressing mode may be used independently, but it is more frequently combined with the File Register, Direct and Indirect Addressing modes. The size of the immediate operand which may be used varies with the instruction type. Constants of size 1-bit (#lit1), 4-bit (#bit4, #lit4 and #Slit4), 5-bit (#lit5), 6-bit (#Slit6), 8-bit (#lit8), 10-bit (#lit10 and #Slit10), 14-bit (#lit14) and 16-bit (#lit16) may be used. Constants may be signed or unsigned and the symbols #Slit4, #Slit6 and #Slit10 designate a signed constant. All other immediate constants are unsigned. Table 4-4 shows the usage of each immediate operand in the instruction set.

Note: The 6-bit (#Slit6) operand is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.

Operand	Instruction Usage	
#lit1	PWRSAV	
#bit4	BCLR, BSET, BTG, BTSC, BTSS, BTST, BTST.C, BTST.Z, BTSTS, BTSTS.C, BTSTS.Z	
#lit4	ASR, LSR, SL	
#Slit4	ADD, LAC, SAC, SAC.R	
#lit5	ADD, ADDC, AND, CP <sup>(5)</sup> , CPB <sup>(5)</sup> , IOR, MUL.SU, MUL.UU, SUB, SUBBR, SUBR, XOR	
#Slit6 <sup>(1)</sup>	SFTAC	
#lit8	MOV.B, CP <sup>(4)</sup> , CPB <sup>(4)</sup>	
#lit10	ADD, ADDC, AND, CP, CPB, IOR, RETLW, SUB, SUBB, XOR	
#Slit10	MOV	
#lit14	DISI, DO <sup>(2)</sup> , LNK, REPEAT <sup>(5)</sup>	
#lit15	D0 <sup>(3)</sup> , REPEAT <sup>(4)</sup>	
#lit16	MOV	

Table 4-4: Immediate Operands in the Instruction Set

**Note 1:** This operand or instruction is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.

- 2: This operand or instruction is only available in dsPIC30F and dsPIC33F devices.
- 3: This operand or instruction is only available in dsPIC33E devices.
- 4: This operand or instruction is only available in dsPIC33E and PIC24E devices.
- **5:** This operand or instruction is only available in dsPIC30F, dsPIC33F, PIC24F, and PIC24H devices.

The syntax for immediate addressing requires that the number sign (#) must immediately precede the constant operand value. The "#" symbol indicates to the assembler that the quantity is a constant. If an out-of-range constant is used with an instruction, the assembler will generate an error. Several examples of immediate addressing are shown in Example 4-7.

Example 4-7: Immediate Addressing

PWRSAV #1	; Enter IDLE mode
ADD.B #0x10, W0	; Add 0x10 to W0 (byte mode)
Before Instruction:	
W0 = 0×12A9	
After Instruction:	
W0 = 0×12B9	
XOR W0, #1, [W1++]	; Exclusive-OR WO and Ox1 ; Store the result to [W1] ; Post-increment W1
Before Instruction:	
WO = 0xFFFF W1 = 0x0890 Data Memory 0x0890 = 0x0032	
After Instruction:	
WO = 0xFFFF W1 = 0x0892 Data Memory 0x0890 = 0xFFFE	

## 4.1.5 Data Addressing Mode Tree

The Data Addressing modes of the PIC24F, PIC24H, and PIC24E families are summarized in Figure 4-1.

	Immediate	
	File Register	No Modification
Data Addressing Modes	Direct	Pre-Increment
	Direct	Pre-Decrement
	Indirect	Post-Increment
		Post-Decrement
		Literal Offset
		Register Offset

Figure 4-1: Data Addressing Mode Tree (PIC24F, PIC24H, and PIC24E)

The Data Addressing modes of the dsPIC30F, dsPIC33F, and dsPIC33E are summarized in Figure 4-2.



Figure 4-2: Data Addressing Mode Tree (dsPIC30F, dsPIC33F, and dsPIC33E)

# 4.2 PROGRAM ADDRESSING MODES

The 16-bit MCU and DSC devices have a 24-bit Program Counter (PC). The PC addresses the 24-bit wide program memory to fetch instructions for execution, and it may be loaded in several ways. For byte compatibility with the table read and table write instructions, each instruction word consumes two locations in program memory. This means that during serial execution, the PC is loaded with PC + 2.

Several methods may be used to modify the PC in a non-sequential manner, and both absolute and relative changes may be made to the PC. The change to the PC may be from an immediate value encoded in the instruction, or a dynamic value contained in a working register. In dsPIC30F, dsPIC33F, and dsPIC33E devices, when D0 looping is active, the PC is loaded with the address stored in the DOSTART register, after the instruction at the DOEND address is executed. For exception handling, the PC is loaded with the address of the exception handler, which is stored in the interrupt vector table. When required, the software stack is used to return scope to the foreground process from where the change in program flow occurred.

Table 4-5 summarizes the instructions which modify the PC. When performing function calls, it is recommended that RCALL be used instead of CALL, since RCALL only consumes 1 word of program memory.

Condition/Instruction	PC Modification	Software Stack Usage
Sequential Execution	PC = PC + 2	None
BRA Expr <sup>(1)</sup> (Branch Unconditionally)	PC = PC + 2*Slit16	None
BRA Condition, Expr <sup>(1)</sup> (Branch Conditionally)	PC = PC + 2 (condition false) PC = PC + 2 * Slit16 (condition true)	None
CALL Expr <sup>(1)</sup> (Call Subroutine)	PC = lit23	PC + 4 is PUSHed on the stack <sup>(2)</sup>
CALL Wn (Call Subroutine Indirect)	PC = Wn	PC + 2 is PUSHed on the stack <sup>(2)</sup>
CALL.L Wn <sup>(5)</sup> (Call Indirect Subroutine Long)	PC = {Wn+1:Wn}	None
GOTO Expr <sup>(1)</sup> (Unconditional Jump)	PC = lit23	None
GOTO Wn (Unconditional Indirect Jump)	PC = Wn	None
GOTO.L Wn <sup>(5)</sup> (Unconditional Indirect Long Jump)	PC = {Wn+1:Wn}	None
RCALL Expr <sup>(1)</sup> (Relative Call)	PC = PC + 2 * Slit16	PC + 2 is PUSHed on the stack <sup>(2)</sup>
RCALL Wn (Computed Relative Call)	PC = PC + 2 * Wn	PC + 2 is PUSHed on the stack <sup>(2)</sup>
Exception Handling	PC = address of the exception handler (read from vector table)	PC + 2 is PUSHed on the stack <sup>(3)</sup>
PC = Target REPEAT instruction (REPEAT Looping)	PC not modified (if REPEAT active)	None
PC = DOEND address <sup>(4)</sup> (D0 Looping)	PC = DOSTART (if D0 active)	None

### Table 4-5: Methods of Modifying Program Flow

Note 1: For BRA, CALL and GOTO, the Expr may be a label, absolute address, or expression, which is resolved by the linker to a 16-bit or 23-bit value (Slit16 or lit23). See Section 5. "Instruction Descriptions" for details.

2: After CALL or RCALL is executed, RETURN or RETLW will POP the Top-of-Stack (TOS) back into the PC.

3: After an exception is processed, RETFIE will POP the Top-of-Stack (TOS) back into the PC.

4: This condition/instruction is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.

5: This condition instruction is only available in dsPIC33E and PIC24E devices.

# 4.3 INSTRUCTION STALLS

In order to maximize the data space EA calculation and operand fetch time, the X data space read and write accesses are partially pipelined. A consequence of this pipelining is that address register data dependencies may arise between successive read and write operations using common registers.

'Read After Write' (RAW) dependencies occur across instruction boundaries and are detected by the hardware. An example of a RAW dependency would be a write operation that modifies W5, followed by a read operation that uses W5 as an Address Pointer. The contents of W5 will not be valid for the read operation until the earlier write completes. This problem is resolved by stalling the instruction execution for one instruction cycle, which allows the write to complete before the next read is started.

# 4.3.1 RAW Dependency Detection

During the instruction pre-decode, the core determines if any address register dependency is imminent across an instruction boundary. The stall detection logic compares the W register (if any) used for the destination EA of the instruction currently being executed with the W register to be used by the source EA (if any) of the prefetched instruction. When a match between the destination and source registers is identified, a set of rules are applied to decide whether or not to stall the instruction by one cycle. Table 4-6 lists various RAW conditions which cause an instruction execution stall.

Destination Address Mode Using Wn	Source Address Mode Using Wn	Stall Required?	Examples <sup>(2)</sup> (Wn = W2)
Direct	Direct	No Stall	ADD.W W0, W1, W2 MOV.W W2, W3
Indirect	Direct	No Stall	ADD.W W0, W1, [W2] MOV.W W2, W3
Indirect	Indirect	No Stall	ADD.W W0, W1, [W2] MOV.W [W2], W3
Indirect	Indirect with pre/post-modification	No Stall	ADD.W W0, W1, [W2] MOV.W [W2++], W3
Indirect with pre/post-modification	Direct	No Stall	ADD.W W0, W1, [W2++] MOV.W W2, W3
Direct	Indirect	Stall <sup>(1)</sup>	ADD.W W0, W1, W2 MOV.W [W2], W3
Direct	Indirect with pre/post-modification	Stall <sup>(1)</sup>	ADD.W W0, W1, W2 MOV.W [W2++], W3
Indirect	Indirect	Stall <sup>(1)</sup>	ADD.W W0, W1, [W2](2) MOV.W [W2], W3(2)
Indirect	Indirect with pre/post-modification	Stall <sup>(1)</sup>	ADD.W W0, W1, [W2](2) MOV.W [W2++], W3(2)
Indirect with pre/post-modification	Indirect	Stall <sup>(1)</sup>	ADD.W W0, W1, [W2++] MOV.W [W2], W3
Indirect with pre/post-modification	Indirect with pre/post-modification	Stall <sup>(1)</sup>	ADD.W W0, W1, [W2++] MOV.W [W2++], W3

Table 4-6: Raw Dependency Rules (Detection By Hardware)

**Note 1:** When stalls are detected, one cycle is added to the instruction execution time.

2: For these examples, the contents of W2 = the mapped address of W2 (0x0004).

## 4.3.2 Instruction Stalls and Exceptions

In order to maintain deterministic operation, instruction stalls are allowed to happen, even if they occur immediately prior to exception processing.

## 4.3.3 Instruction Stalls and Instructions that Change Program Flow

CALL and RCALL write to the stack using W15 and may, therefore, be subject to an instruction stall if the source read of the subsequent instruction uses W15.

GOTO, RETFIE and RETURN instructions are never subject to an instruction stall because they do not perform write operations to the working registers.

## 4.3.4 Instruction Stalls and DO/REPEAT Loops

Instructions operating in a D0 or REPEAT loop are subject to instruction stalls, just like any other instruction. Stalls may occur on loop entry, loop exit and also during loop processing.

Note: D0 loops are only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.

## 4.3.5 Instruction Stalls and PSV

Instructions operating in PSV address space are subject to instruction stalls, just like any other instruction. Should a data dependency be detected in the instruction immediately following the PSV data access, the second cycle of the instruction will initiate a stall. Should a data dependency be detected in the instruction immediately before the PSV data access, the last cycle of the previous instruction will initiate a stall.

**Note:** Refer to the specific device family reference manual for more detailed information about RAW instruction stalls.

## 4.4 BYTE OPERATIONS

Since the data memory is byte addressable, most of the base instructions may operate in either Byte mode or Word mode. When these instructions operate in Byte mode, the following rules apply:

- All direct working register references use the Least Significant Byte of the 16-bit working register and leave the Most Significant Byte (MSB) unchanged
- All indirect working register references use the data byte specified by the 16-bit address stored in the working register
- · All file register references use the data byte specified by the byte address
- · The STATUS Register is updated to reflect the result of the byte operation

It should be noted that data addresses are always represented as **byte** addresses. Additionally, the native data format is little-endian, which means that words are stored with the Least Significant Byte at the lower address, and the Most Significant Byte at the adjacent, higher address (as shown in Figure 4-3). Example 4-8 shows sample byte move operations and Example 4-9 shows sample byte math operations.

**Note:** Instructions that operate in Byte mode must use the ".b" or ".B" instruction extension to specify a byte instruction. For example, the following two instructions are valid forms of a byte clear operation:

- CLR.b W0
- CLR.B W0

#### Example 4-8: Sample Byte Move Operations

```
MOV.B #0x30, W0
                                 ; move the literal byte 0x30 to W0
Before Instruction:
    W0 = 0 \times 5555
After Instruction:
    W0 = 0 \times 5530
    MOV.B 0x1000, W0
                                 ; move the byte at 0x1000 to W0
Before Instruction:
    W0 = 0 \times 5555
    Data Memory 0 \times 1000 = 0 \times 1234
After Instruction:
    W0 = 0 \times 5534
    Data Memory 0 \times 1000 = 0 \times 1234
    MOV.B W0, 0x1001
                                 ; byte move W0 to address 0x1001
Before Instruction:
    W0 = 0 \times 1234
    Data Memory 0 \times 1000 = 0 \times 5555
After Instruction:
    W0 = 0 \times 1234
    Data Memory 0 \times 1000 = 0 \times 3455
                                ; byte move W0 to [W1], then post-inc W1
    MOV.B W0, [W1++]
Before Instruction:
    W0 = 0 \times 1234
    W1 = 0 \times 1001
    Data Memory 0 \times 1000 = 0 \times 5555
After Instruction:
    W0 = 0 \times 1234
    W1 = 0 \times 1002
    Data Memory 0 \times 1000 = 0 \times 3455
```

```
CLR.B
            [W6--]
                                     ; byte clear [W6], then post-dec W6
Before Instruction:
    W6 = 0 \times 1001
    Data Memory 0 \times 1000 = 0 \times 5555
After Instruction:
    W6 = 0 \times 1000
    Data Memory 0 \times 1000 = 0 \times 0055
                                   ; byte subtract literal 0x10 from W0
    SUB.B W0, #0x10, W1
                                     ; and store to W1
Before Instruction:
    W0 = 0 \times 1234
    W1 = 0xFFFF
After Instruction:
    W0 = 0 \times 1234
    W1 = 0 \times FF24
    ADD.B W0, W1, [W2++]
                                   ; byte add W0 and W1, store to [W2]
                                     ; and post-inc W2
Before Instruction:
    W0 = 0 \times 1234
    W1 = 0 \times 5678
    W2 = 0 \times 1000
    Data Memory 0 \times 1000 = 0 \times 5555
After Instruction:
    W0 = 0 \times 1234
    W1 = 0 \times 5678
    W2 = 0x1001
    Data Memory 0x1000 = 0x55AC
```

Example 4-9: Sample Byte Math Operations

ion Set ils

# 4.5 WORD MOVE OPERATIONS

Even though the data space is byte addressable, all move operations made in Word mode must be word-aligned. This means that for all source and destination operands, the Least Significant address bit must be '0'. If a word move is made to or from an odd address, an address error exception is generated. Likewise, all double words must be word-aligned. Figure 4-3 shows how bytes and words may be aligned in data memory. Example 4-10 contains several legal word move operations.

When an exception is generated due to a misaligned access, the exception is taken after the instruction executes. If the illegal access occurs from a data read, the operation will be allowed to complete, but the Least Significant bit of the source address will be cleared to force word alignment. If the illegal access occurs during a data write, the write will be inhibited. Example 4-11 contains several illegal word move operations.

			_				
0x100	1	b0	0x1000				
0x100	3 <b>b1</b>		0x1002				
0x100	5 <b>b3</b>	b2	0x1004				
0x100	7 <b>b5</b>	b4	0x1006				
0x100	9 <b>b7</b>	b6	0x1008				
0x100	в	b8	0x100A				
Legend: b0 – byte stored at 0x1000 b1 – byte stored at 0x1003 b3:b2 – word stored at 0x1005:1004 (b2 is LSB) b7:b4 – double word stored at 0x1009:0x1006 (b4 is LSB) b8 – byte stored at 0x100A							
<b>Note:</b> Instructions that operate in Word mode are not required to use an instruction extension. However, they may be specified with an optional ".w" or ".W" extension, if desired. For example, the following instructions are valid forms of a word clear operation:							

Figure 4-3: Data Alignment in Memory

ор	eration:	
•	CLR W0	

- CLR.w W0
- CLR.W W0

Example 4-10: Legal Word Move Operations

Example 4-1	U. Ley	ai wort		perai	10115						
MOV	#0x30,	WO	;	move	the	litera	al	word	0x30	to	WO
Before Instru	ction:										
WO = OX	5555										
After Instruct	ion:										
W0 = 0×	0030										
MOV	0×1000,	WO	;	move	the	word a	at	0x100	90 to	WO	
Before Instru	ction:										
WO = Ox Data Me	5555 mory 0x:	1000 =	0x1234								
After Instruct	ion:										
WO = Ox Data Me	1234 mory 0x:	1000 =	0x1234								
	[W0], [	W1++]				e [WO] :-inc W		[W1]	],		
Before Instru	ction:										
After Instruct	ion:										
baca ne			2700000								

```
; move the word at 0x1001 to W0
    MOV
              0x1001, W0
Before Instruction:
W0 = 0x5555
Data Memory 0 \times 1000 = 0 \times 1234
Data Memory 0 \times 1002 = 0 \times 5678
After Instruction:
W0 = 0 \times 1234
Data Memory 0 \times 1000 = 0 \times 1234
Data Memory 0 \times 1002 = 0 \times 5678
ADDRESS ERROR TRAP GENERATED
(source address is misaligned, so MOV is performed)
    MOV
             W0, 0x1001
                                     ; move W0 to the word at 0x1001
Before Instruction:
W0 = 0 \times 1234
Data Memory 0 \times 1000 = 0 \times 5555
Data Memory 0 \times 1002 = 0 \times 6666
After Instruction:
W0 = 0 \times 1234
Data Memory 0 \times 1000 = 0 \times 5555
Data Memory 0 \times 1002 = 0 \times 6666
ADDRESS ERROR TRAP GENERATED
(destination address is misaligned, so MOV is not performed)
    MOV
              [W0], [W1++]
                                     ; word move [W0] to [W1],
                                     ; then post-inc W1
Before Instruction:
W0 = 0 \times 1235
W1 = 0 \times 1000
Data Memory 0 \times 1000 = 0 \times 1234
Data Memory 0x1234 = 0xAAAA
Data Memory 0x1236 = 0xBBBB
After Instruction:
W0 = 0 \times 1235
W1 = 0 \times 1002
Data Memory 0x1000 = 0xAAAA
Data Memory 0x1234 = 0xAAAA
Data Memory 0x1236 = 0xBBBB
ADDRESS ERROR TRAP GENERATED
(source address is misaligned, so MOV is performed)
```

Example 4-11: Illegal Word Move Operations

# 4.6 USING 10-BIT LITERAL OPERANDS

Several instructions that support Byte and Word mode have 10-bit operands. For byte instructions, a 10-bit literal is too large to use. So when 10-bit literals are used in Byte mode, the range of the operand must be reduced to 8 bits or the assembler will generate an error. Table 4-7 shows that the range of a 10-bit literal is 0:1023 in Word mode and 0:255 in Byte mode.

Instructions which employ 10-bit literals in Byte and Word mode are: ADD, ADDC, AND, IOR, RETLW, SUB, SUBB, and XOR. Example 4-12 shows how positive and negative literals are used in Byte mode for the ADD instruction.

Literal Value	Word Mode kk kkkk kkkk	<b>Byte Mode</b> kkkk kkkk		
0	00 0000 0000	0000 0000		
1	00 0000 0001	0000 0001		
2	00 0000 0010	0000 0010		
127	00 0111 1111	0111 1111		
128	00 1000 0000	1000 0000		
255	00 1111 1111	1111 1111		
256	01 0000 0000	N/A		
512	10 0000 0000	N/A		
1023	11 1111 1111	N/A		

Table 4-7: 10-bit Literal Coding

### Example 4-12: Using 10-bit Literals for Byte Operands

ADD.B	#0x80, W0	; add 128 (or -128) to W0
ADD.B	#0x380, W0	; ERROR Illegal syntax for byte mode
ADD.B	#0×FF, W0	; add 255 (or -1) to W0
ADD.B	#0x3FF, W0	; ERROR Illegal syntax for byte mode
ADD.B	#0×F, W0	; add 15 to WO
ADD.B	#0x7F, W0	; add 127 to W0
ADD.B	#0x100, W0	; ERROR Illegal syntax for byte mode

**Note:** Using a literal value greater than 127 in Byte mode is functionally identical to using the equivalent negative two's complement value, since the Most Significant bit of the byte is set. When operating in Byte mode, the Assembler will accept either a positive or negative literal value (i.e., #-10).

# 4.7 SOFTWARE STACK POINTER AND FRAME POINTER

## 4.7.1 Software Stack Pointer

The 16-bit MCU and DSC devices feature a software stack which facilitates function calls and exception handling. W15 is the default Stack Pointer (SP) and after any Reset, it is initialized to 0x0800 (0x1000 for PIC24E and dsPIC33E devices). This ensures that the SP will point to valid RAM and permits stack availability for exceptions, which may occur before the SP is set by the user software. The user may reprogram the SP during initialization to any location within data space.

The SP always points to the first available free word (Top-of-Stack) and fills the software stack, working from lower addresses towards higher addresses. It pre-decrements for a stack POP (read) and post-increments for a stack PUSH (write).

The software stack is manipulated using the PUSH and POP instructions. The PUSH and POP instructions are the equivalent of a MOV instruction, with W15 used as the destination pointer. For example, the contents of W0 can be PUSHed onto the Top-of-Stack (TOS) by:

PUSH W0

This syntax is equivalent to:

MOV W0, [W15++]

The contents of the TOS can be returned to W0 by:

POP W0

This syntax is equivalent to:

MOV [--W15],W0

During any CALL instruction, the PC is PUSHed onto the stack, such that when the subroutine completes execution, program flow may resume from the correct location. When the PC is PUSHed onto the stack, PC<15:0> is PUSHed onto the first available stack word, then PC<22:16> is PUSHed. When PC<22:16> is PUSHed, the Most Significant 7 bits of the PC are zero-extended before the PUSH is made, as shown in Figure 4-4. During exception processing, the Most Significant 7 bits of the PC are concatenated with the lower byte of the STATUS register (SRL) and IPL<3>, CORCON<3>. This allows the primary STATUS register contents and CPU Interrupt Priority Level to be automatically preserved during interrupts.

Note: In order to protect against misaligned stack accesses, W15<0> is always clear.

Figure 4-4: Stack Operation for CALL Instruction



### 4.7.1.1 STACK POINTER EXAMPLE

Figure 4-5 through Figure 4-8 show how the software stack is modified for the code snippet shown in Example 4-13. Figure 4-5 shows the software stack before the first PUSH has executed. Note that the SP has the initialized value of 0x0800. Furthermore, the example loads 0x5A5A and 0x3636 to W0 and W1, respectively. The stack is PUSHed for the first time in Figure 4-6 and the value contained in W0 is copied to TOS. W15 is automatically updated to point to the next available stack location, and the new TOS is 0x0802. In Figure 4-7, the contents of W1 are PUSHed onto the stack, and the new TOS becomes 0x0804. In Figure 4-8, the stack is POPped, which copies the last PUSHed value (W1) to W3. The SP is decremented during the POP operation, and at the end of the example, the final TOS is 0x0802.

#### Example 4-13: Stack Pointer Usage

-		-	
MOV	#0x5A5A, W0	; Load W0 with 0x5A5A	
MOV	#0x3636, W1	; Load W1 with 0x3636	
PUSH	WO	; Push W0 to TOS (see Figure 4-5)	
PUSH	W1	; Push W1 to TOS (see Figure 4-7)	
POP	W3	; Pop TOS to W3 (see Figure 4-8)	

















## 4.7.2 Software Stack Frame Pointer

A Stack Frame is a user-defined section of memory residing in the software stack. It is used to allocate memory for temporary variables which a function uses, and one Stack Frame may be created for each function. W14 is the default Stack Frame Pointer (FP) and it is initialized to 0x0000 on any Reset. If the Stack Frame Pointer is not used, W14 may be used like any other working register.

The link (LNK) and unlink (ULNK) instructions provide Stack Frame functionality. The LNK instruction is used to create a Stack Frame. It is used during a call sequence to adjust the SP, such that the stack may be used to store temporary variables utilized by the called function. After the function completes execution, the ULNK instruction is used to remove the Stack Frame created by the LNK instruction. The LNK and ULNK instructions must always be used together to avoid stack overflow.
### 4.7.2.1 STACK FRAME POINTER EXAMPLE

Figure 4-9 through Figure 4-11 show how a Stack Frame is created and removed for the code snippet shown in Example 4-14. This example demonstrates how a Stack Frame operates and is not indicative of the code generated by the compiler. Figure 4-9 shows the stack condition at the beginning of the example, before any registers are pushed to the stack. Here, W15 points to the first free stack location (TOS) and W14 points to a portion of stack memory allocated for the routine that is currently executing.

Before calling the function "COMPUTE", the parameters of the function (W0, W1 and W2) are PUSHed on the stack. After the "CALL COMPUTE" instruction is executed, the PC changes to the address of "COMPUTE" and the return address of the function "TASKA" is placed on the stack (Figure 4-10). Function "COMPUTE" then uses the "LNK #4" instruction to PUSH the calling routine's Frame Pointer value onto the stack and the new Frame Pointer will be set to point to the current Stack Pointer. Then, the literal 4 is added to the Stack Pointer address in W15, which reserves memory for two words of temporary data (Figure 4-11).

Inside the function "COMPUTE", the FP is used to access the function parameters and temporary (local) variables. [W14 + n] will access the temporary variables used by the routine and [W14 - n] is used to access the parameters. At the end of the function, the ULNK instruction is used to copy the Frame Pointer address to the Stack Pointer and then POP the calling subroutine's Frame Pointer back to the W14 register. The ULNK instruction returns the stack back to the state shown in Figure 4-10.

A RETURN instruction will return to the code that called the subroutine. The calling code is responsible for removing the parameters from the stack. The RETURN and POP instructions restore the stack to the state shown in Figure 4-9.

Example 4-14: Frame Pointer Usage

TASKA:	
PUSH W0	; Push parameter 1
PUSH W1	; Push parameter 2
PUSH W2	; Push parameter 3
CALL COMPU	TE ; Call COMPUTE function
POP W2	; Pop parameter 3
POP W1	; Pop parameter 2
POP WO	; Pop parameter 1
COMPUTE:	
LNK #4	; Stack FP, allocate 4 bytes for local variables
ULNK	; Free allocated memory, restore original FP
RETURN	; Return to TASKA













### 4.7.3 Stack Pointer Overflow

There is a Stack Limit register (SPLIM) associated with the Stack Pointer that is reset to 0x0000. SPLIM is a 16-bit register, but SPLIM<0> is fixed to '0', because all stack operations must be word-aligned.

The stack overflow check will not be enabled until a word write to SPLIM occurs, after which time it can only be disabled by a device Reset. All effective addresses generated using W15 as a source or destination are compared against the value in SPLIM. Should the effective address be greater than the contents of SPLIM, then a stack error trap is generated.

If stack overflow checking has been enabled, a stack error trap will also occur if the W15 effective address calculation wraps over the end of data space (0xFFFF).

Refer to the specific device family reference manual for more information on the stack error trap.

### 4.7.4 Stack Pointer Underflow

The stack is initialized to 0x0800 during Reset (0x1000 for PIC24E and dsPIC33E devices). A stack error trap will be initiated should the Stack Pointer address ever be less than 0x0800 (0x1000 for PIC24E and dsPIC33E devices).

Note:	Locations in data space between 0x0000 and 0x07FF (0x0FFF for PIC24E and
	dsPIC33E devices) are, in general, reserved for core and peripheral Special
	Function Registers (SFRs).

## 4.7.5 Stack Frame Active (SFA) Control (dsPIC33E and PIC24E Devices)

W15 is never subject to paging and is therefore restricted to address range 0x000000 to 0x00FFFF. However, the Stack Frame Pointer (W14) for any user software function is only dedicated to that function when a stack frame addressed by W14 is active (i.e., after a LNK instruction). Therefore, it is desirable to have the ability to dynamically switch W14 between use as a general purpose W register, and use as a Stack Frame Pointer. The SFA Status bit (CORCON<2>) achieves this function without additional software overhead.

When the SFA bit is clear, W14 may be used with any page register. When SFA is set, W14 is not subject to paging and is locked into the same address range as W15 (0x000000 to 0x00FFFF). Operation of the SFA register lock is as follows:

- The LNK instruction sets SFA (and creates a stack frame)
- The ULNK instruction clears SFA (and deletes the stack frame)
- The CALL, CALL. L, and RCALL instructions also stack the SFA bit (placing it in the LSb of the stacked PC), and clear the SFA bit after the stacking operation is complete. The called procedure is now free to either use W14 as a general purpose register, or create another stack frame using the LNK instruction.
- The RETURN, RETLW and RETFIE instructions all restore the SFA bit from its previously stacked value

The SFA bit is a read-only bit. It can only be set by execution of the LNK instruction, and cleared by the ULNK, CALL, CALL. L, and RCALL instructions.

Note: In dsPIC33E and PIC24E devices, the SFA bit is stacked instead of PC<0>.

#### 4.8 **CONDITIONAL BRANCH INSTRUCTIONS**

Conditional branch instructions are used to direct program flow, based on the contents of the STATUS register. These instructions are generally used in conjunction with a Compare class instruction, but they may be employed effectively after any operation that modifies the STATUS register.

The compare instructions CP, CP0 and CPB, perform a subtract operation (minuend - subtrahend), but do not actually store the result of the subtraction. Instead, compare instructions just update the flags in the STATUS register, such that an ensuing conditional branch instruction may change program flow by testing the contents of the updated STATUS register. If the result of the STATUS register test is true, the branch is taken. If the result of the STATUS register test is false, the branch is not taken.

The conditional branch instructions supported by the dsPIC30F, dsPIC33F, and dsPIC33E devices are shown in Table 4-8. This table identifies the condition in the STATUS register which must be true for the branch to be taken. In some cases, just a single bit is tested (as in BRA C), while in other cases, a complex logic operation is performed (as in BRA GT). For dsPIC30F, dsPIC33F, and dsPIC33E devices, it is worth noting that both signed and unsigned conditional tests are supported, and that support is provided for DSP algorithms with the OA, OB, SA and SB condition mnemonics.

Condition Mnemonic <sup>(1)</sup>	Description	Status Test
С	Carry (not Borrow)	С
GE	Signed greater than or equal	(N&&OV)    (N&&OV)
GEU <sup>(2)</sup>	Unsigned greater than or equal	С
GT	Signed greater than	(Z&&N&&OV)    (Z&&N&&OV)
GTU	Unsigned greater than	C&&Z
LE	Signed less than or equal	Z    (N&&OV)    (N&&OV)
LEU	Unsigned less than or equal	<u>¯</u> ∥ z
LT	Signed less than	(N&&OV)    (N&&OV)
LTU <sup>(3)</sup>	Unsigned less than	С
N	Negative	N
NC	Not Carry (Borrow)	С
NN	Not Negative	N
NOV	Not Overflow	OV
NZ	Not Zero	Z
0A <sup>(4)</sup>	Accumulator A overflow	OA
OB <sup>(4)</sup>	Accumulator B overflow	ОВ
OV	Overflow	OV
SA <sup>(4)</sup>	Accumulator A saturate	SA
SB <sup>(4)</sup>	Accumulator B saturate	SB
Z	Zero	Z

#### Table 4-8: **Conditional Branch Instructions**

**Note 1:** Instructions are of the form: BRA mnemonic, Expr.

**2:** GEU is identical to C and will reverse assemble to BRA C, Expr.

LTU is identical to NC and will reverse assemble to BRA NC, Expr. 3:

This condition is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices. 4:

Note: The "Compare and Skip" instructions (CPBEQ, CPBGT, CPBLT, CPBNE, CPSEQ, CPSGT, CPSLT, and CPSNE) do not modify the STATUS register.

### 4.9 Z STATUS BIT

The Z Status bit is a special zero Status bit that is useful for extended precision arithmetic. The Z bit functions like a normal Z flag for all instructions, except those that use the Carry/Borrow input (ADDC, CPB, SUBB and SUBBR). For the ADDC, CPB, SUBB and SUBBR instructions, the Z bit can only be cleared and never set. If the result of one of these instructions is non-zero, the Z bit will be cleared and will remain cleared, regardless of the result of subsequent ADDC, CPB, SUBB or SUBBR operations. This allows the Z bit to be used for performing a simple zero check on the result of a series of extended precision operations.

A sequence of instructions working on multi-precision data (starting with an instruction with no Carry/Borrow input), will automatically logically AND the successive results of the zero test. All results must be zero for the Z flag to remain set at the end of the sequence of operations. If the result of the ADDC, CPB, SUBB or SUBBR instruction is non-zero, the Z bit will be cleared and remain cleared for all subsequent ADDC, CPB, SUBB or SUBBR or SUBBR instructions. Example 4-15 shows how the Z bit operates for a 32-bit addition. It shows how the Z bit is affected for a 32-bit addition implemented with an ADD/ADDC instruction sequence. The first example generates a zero result for only the most significant word, and the second example generates a zero result for both the least significant word and most significant word.



Example 4-15: 2 Status bit Operation for 32-bit Addition
; Add two doubles (W0:W1 and W2:W3)
; Store the result in W5:W4
ADD W0, W2, W4 ; Add LSWord and store to W4 ADDC W1, W3, W5 ; Add MSWord and store to W5
ADDC W1, W3, W5 ; Add MSWord and store to W5
Before 32-bit Addition (zero result for the most significant word):
$W0 = 0 \times 2342$
W1 = 0xFFF0
$W2 = 0 \times 39 A A$
$W_2 = 0.00010$ W3 = 0.00010
$W4 = 0 \times 0000$
$W5 = 0 \times 0000$
$SR = 0 \times 0000$
After 32-bit Addition:
W0 = 0x2342
W1 = 0×FFF0
W2 = 0x39AA
$W3 = 0 \times 0010$
W4 = 0×5CEC
$W5 = 0 \times 0000$
$SR = 0 \times 0201 (DC, C=1)$
Before 32-bit Addition (zero result for the least significant word and most significant word):
W0 = 0×B76E
W1 = 0×FB7B
W2 = 0×4892
$W3 = 0 \times 0484$
$W4 = 0 \times 0000$
$W5 = 0 \times 0000$
$SR = 0 \times 0000$
After 32-bit Addition:
$W0 = 0 \times B76E$
W1 = 0xFB7B
$W2 = 0 \times 4892$
$W3 = 0 \times 0485$
$W4 = 0 \times 0000$
$W5 = 0 \times 0000$
SR = 0x0103 (DC,Z,C=1)

### 4.10 ASSIGNED WORKING REGISTER USAGE

The 16 working registers of the 16-bit MCU and DSC devices provide a large register set for efficient code generation and algorithm implementation. In an effort to maintain an instruction set that provides advanced capability, a stable run-time environment and backwards compatibility with earlier Microchip processor cores, some working registers have a preassigned usage. Table 4-9 summarizes these working register assignments. For the dsPIC30F, dsPIC33F, and dsPIC33E, additional details are provided in subsections Section 4.10.1 "Implied DSP Operands (dsPIC30F, dsPIC33F and dsPIC33E Devices)" through Section 4.10.3 "PIC<sup>®</sup> Microcontroller Compatibility".

Register	Special Assignment	
W0	Default WREG, Divide Quotient	
W1	Divide Remainder	
W2	"MUL f" Product least significant word	
W3	"MUL f" Product most significant word	
W4	MAC Operand <sup>(1)</sup>	
W5	MAC Operand <sup>(1)</sup>	
W6	MAC Operand <sup>(1)</sup>	
W7	MAC Operand <sup>(1)</sup>	
W8	MAC Prefetch Address (X Memory) <sup>(1)</sup>	
W9	MAC Prefetch Address (X Memory) <sup>(1)</sup>	
W10	MAC Prefetch Address (Y Memory) <sup>(1)</sup>	
W11	MAC Prefetch Address (Y Memory) <sup>(1)</sup>	
W12	MAC Prefetch Offset <sup>(1)</sup>	
W13	MAC Write Back Destination <sup>(1)</sup>	
W14	Frame Pointer	
W15	Stack Pointer	

 Table 4-9:
 Special Working Register Assignments

Note 1: This assignment is only applicable in dsPIC30F, dsPIC33F, and dsPIC33E devices.

## 4.10.1 Implied DSP Operands (dsPIC30F, dsPIC33F and dsPIC33E Devices)

To assist instruction encoding and maintain uniformity among the DSP class of instructions, some working registers have pre-assigned functionality. For all DSP instructions which have prefetch ability, the following 10 register assignments must be adhered to:

- W4-W7 are used for arithmetic operands
- · W8-W11 are used for prefetch addresses (pointers)
- · W12 is used for the prefetch register offset index
- W13 is used for the accumulator Write Back destination

These restrictions only apply to the DSP MAC class of instructions, which utilize working registers and have prefetch ability (described in Section 4.15 "DSP Accumulator Instructions (dsPIC30F, dsPIC33F and dsPIC33E Devices)"). These instructions are CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY . N and MSC.

In dsPIC33E devices, mixed-sign DSP multiplication operations are supported without the need to dynamically modify the US<1:0> bits. In this mode (US<1:0> = '10'), each input operand is treated as unsigned or signed based on which register is being used for that operand. W4 and W6 are always unsigned operand, whereas W5 and W7 are always signed operands. This feature can be used to efficiently execute extended-precision DSP multiplications.

The DSP Accumulator class of instructions (described in **Section 4.15 "DSP Accumulator Instructions (dsPIC30F, dsPIC33F and dsPIC33E Devices)**") are not required to follow the working register assignments in Table 4-9 and may freely use any working register when required.

### 4.10.2 Implied Frame and Stack Pointer

To accommodate software stack usage, W14 is the implied Frame Pointer (used by the LNK and ULNK instructions) and W15 is the implied Stack Pointer (used by the CALL, LNK, POP, PUSH, RCALL, RETFIE, RETLW, RETURN, TRAP and ULNK instructions). Even though W14 and W15 have this implied usage, they may still be used as generic operands in any instruction, with the exceptions outlined in **Section 4.10.1 "Implied DSP Operands (dsPIC30F, dsPIC33F and dsPIC33E Devices)**". If W14 and W15 must be used for other purposes (it is strongly advised that they remain reserved for the Frame and Stack Pointer), extreme care must be taken such that the run-time environment is not corrupted.

### 4.10.3 PIC<sup>®</sup> Microcontroller Compatibility

### 4.10.3.1 DEFAULT WORKING REGISTER WREG

To ease the migration path for users of the Microchip 8-bit PIC MCU families, the 16-bit MCU and DSC devices have matched the functionality of the PIC MCU instruction sets as closely as possible. One major difference between the 16-bit MCU and DSC and the 8-bit PIC MCU processors is the number of working registers provided. The 8-bit PIC MCU families only provide one 8-bit working register, while the 16-bit MCU and DSC families provide sixteen, 16-bit working registers. To accommodate for the one working register of the 8-bit PIC MCU, the 16-bit MCU and DSC device instruction set has designated one working register to be the default working register for all legacy file register instructions. The default working register is set to W0, and it is used by all instructions which use file register addressing.

Additionally, the syntax used by the 16-bit MCU and DSC device assembler to specify the default working register is similar to that used by the 8-bit PIC MCU assembler. As shown in the detailed instruction descriptions in **Section 5. "Instruction Descriptions"**, "WREG" must be used to specify the default working register. Example 4-16 shows several instructions that use WREG.

### Example 4-16: Using the Default Working Register WREG

ADD	RAM100	; add RAM100 and WREG, store in RAM100
ASR	RAM100, WREG	; shift RAM100 right, store in WREG
CLR.B	WREG	; clear the WREG LS Byte
DEC	RAM100, WREG	; decrement RAM100, store in WREG
MOV	WREG, RAM100	; move WREG to RAM100
SETM	WREG	; set all bits in the WREG
XOR	RAM100	; XOR RAM100 and WREG, store in RAM100

### 4.10.3.2 PRODH:PRODL REGISTER PAIR

Another significant difference between the Microchip 8-bit PIC MCU and 16-bit MCU and DSC architectures is the multiplier. Some PIC MCU families support an 8-bit x 8-bit multiplier, which places the multiply product in the PRODH:PRODL register pair. The 16-bit MCU and DSC devices have a 17-bit x 17-bit multiplier, which may place the result into any two successive working registers (starting with an even register), or an accumulator.

Despite this architectural difference, the 16-bit MCU and DSC devices still support the legacy file register multiply instruction (MULWF) with the "MUL{.B} f" instruction (described on page 303). Supporting the legacy MULWF instruction has been accomplished by mapping the PRODH:PRODL registers to the working register pair W3:W2. This means that when "MUL{.B} f" is executed in Word mode, the multiply generates a 32-bit product which is stored in W3:W2, where W3 has the most significant word of the product and W2 has the least significant word of the product. When "MUL{.B} f" is executed in Byte mode, the 16-bit product is stored in W2, and W3 is unaffected. Examples of this instruction are shown in Example 4-17.

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Example 4-17.	onsight	- 4		anapiy	(Leguo)			Straotiony
MUL.B 0x10	00	;	(0x100)*WREG	(byte	mode),	store	to	W2
Before Instruction	:							
W0 (WREG) = W2 = 0x1235 W3 = 0x1000 Data Memory		=	0x1255					
After Instruction:								
W0 (WREG) = W2 = 0×01A9 W3 = 0×1000								
Data Memory	0x0100	=	0x1255					
MUL 0×10	00	;	(0×100)*WREG	(word	mode),	store	to	W3:W2
Before Instruction	:							
W0 (WREG) = W2 = 0x1235 W3 = 0x1000		_	0.1055					
Data Memory After Instruction:	0X0100	=	0X1255					
Alter Instruction:								
W0 (WREG) = W2 = 0×DEA9 W3 = 0×0885								
Data Memory	0x0100	=	0x1255					

#### Example 4-17: Unsigned f and WREG Multiply (Legacy MULWF Instruction)

### 4.10.3.3 MOVING DATA WITH WREG

The "MOV{.B} f {, WREG}" instruction (described on page 279) and "MOV{.B} WREG, f" instruction (described on page 280) allow for byte or word data to be moved between file register memory and the WREG (working register W0). These instructions provide equivalent functionality to the legacy Microchip PIC MCU MOVF and MOVWF instructions.

The "MOV{.B} f {, WREG}" and "MOV{.B} WREG, f" instructions are the only MOV instructions which support moves of byte data to and from file register memory. Example 4-18 shows several MOV instruction examples using the WREG.

Note: When moving word data between file register memory and the working register array, the "MOV Wns, f" and "MOV f, Wnd" instructions allow any working register (W0:W15) to be used as the source or destination register, not just WREG.

### Example 4-18: Moving Data with WREG

MOV.B 0x1001, WREG ; move the byte stored at location 0x1001 to W	10
MOV 0x1000, WREG ; move the word stored at location 0x1000 to W	10
MOV.B WREG, TBLPAG ; move the byte stored at W0 to the TBLPAG reg	jister
MOV WREG, 0x804 ; move the word stored at W0 to location 0x804	ţ

### 4.11 DSP DATA FORMATS (dsPIC30F, dsPIC33F AND dsPIC33E DEVICES)

### 4.11.1 Integer and Fractional Data

The dsPIC30F, dsPIC33F, and dsPIC33E devices support both integer and fractional data types. Integer data is inherently represented as a signed two's complement value, where the Most Significant bit is defined as a sign bit. Generally speaking, the range of an N-bit two's complement integer is  $-2^{N-1}$  to  $2^{N-1} - 1$ . For a 16-bit integer, the data range is -32768 (0x8000) to 32767 (0x7FFF), including '0'. For a 32-bit integer, the data range is -2,147,483,648 (0x8000 0000) to 2,147,483,647 (0x7FFF FFFF).

Fractional data is represented as a two's complement number, where the Most Significant bit is defined as a sign bit, and the radix point is implied to lie just after the sign bit. This format is commonly referred to as 1.15 (or Q15) format, where 1 is the number of bits used to represent the integer portion of the number, and 15 is the number of bits used to represent the fractional portion. The range of an N-bit two's complement fraction with this implied radix point is -1.0 to  $(1 - 2^{1-N})$ . For a 16-bit fraction, the 1.15 data range is -1.0 (0x8000) to 0.999969482 (0x7FFF), including 0.0 and it has a precision of 3.05176x10<sup>-5</sup>. In Normal Saturation mode, the 32-bit accumulators use a 1.31 format, which enhances the precision to 4.6566x10<sup>-10</sup>.

The dynamic range of the accumulators can be expanded by using the 8 bits of the Upper Accumulator register (ACCxU) as guard bits. Guard bits are used if the value stored in the accumulator overflows beyond the  $32^{nd}$  bit, and they are useful for implementing DSP algorithms. This mode is enabled when the ACCSAT bit (CORCON<4>) is set to '1' and it expands the accumulators to 40 bits. The guard bits are also used when the accumulator saturation is disabled. The accumulators then support an integer range of -5.498x10<sup>11</sup> (0x80 0000 0000) to 5.498x10<sup>11</sup> (0x7F FFFF FFFF). In Fractional mode, the guard bits of the accumulator do not modify the location of the radix point and the 40-bit accumulators use a 9.31 fractional format. Note that all fractional operation results are stored in the 40-bit Accumulator, justified with a 1.31 radix point. As in Integer mode, the guard bits merely increase the dynamic range of the accumulator. 9.31 fractions have a range of -256.0 (0x80 0000 0000) to (256.0 – 4.65661x10<sup>-10</sup>) (0x7F FFFF FFFF). Table 4-10 identifies the range and precision of integers and fractions on the dsPIC30F/33F/33E devices for 16-bit, 32-bit and 40-bit registers.

It should be noted that, with the exception of DSP multiplies, the ALU operates identically on integer and fractional data. Namely, an addition of two integers will yield the same result (binary number) as the addition of two fractional numbers. The only difference is how the result is interpreted by the user. However, multiplies performed by DSP operations are different. In these instructions, data format selection is made by the IF bit (CORCON<0>), and it must be set accordingly ('0' for Fractional mode, '1' for Integer mode). This is required because of the implied radix point used by dsPIC30F/33F/33E fractional numbers. In Integer mode, multiplying two 16-bit integers produces a 32-bit integer result. However, multiplying two 1.15 values generates a 2.30 result. Since the dsPIC30F, dsPIC33F, and dsPIC33E devices use a 1.31 format for the accumulators, a DSP multiply in Fractional mode also includes a left shift of one bit to keep the radix point properly aligned. This feature reduces the resolution of the DSP multiplier to  $2^{-30}$ , but has no other effect on the computation (e.g.,  $0.5 \times 0.5 = 0.25$ ).

Register Size	r Size Integer Range Fraction Range		Fraction Resolution
16-bit	-32768 to 32767	-1.0 to (1.0 – 2 <sup>-15</sup> )	3.052 x 10 <sup>-5</sup>
32-bit	-2,147,483,648 to 2,147,483,647		4.657 x 10 <sup>-10</sup>
40-bit	-549,755,813,888 to 549,755,813,887	-256.0 to (256.0 – 2 <sup>-31</sup> )	4.657 x 10 <sup>-10</sup>

Table 4-10: dsPIC30F/33F/33E Data Ranges

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### 4.11.2 Integer and Fractional Data Representation

Having a working knowledge of how integer and fractional data are represented on the dsPIC30F, dsPIC33F, and dsPIC33E is fundamental to working with the device. Both integer and fractional data treat the Most Significant bit as a sign bit, and the binary exponent decreases by one as the bit position advances toward the Least Significant bit. The binary exponent for an N-bit integer starts at (N-1) for the Most Significant bit, and ends at '0' for the Least Significant bit. For an N-bit fraction, the binary exponent starts at '0' for the Most Significant bit, and ends at (1-N) for the Least Significant bit (as shown in Figure 4-12 for a positive value and in Figure 4-13 for a negative value).

Conversion between integer and fractional representations can be performed using simple division and multiplication. To go from an N-bit integer to a fraction, divide the integer value by  $2^{N-1}$ . Similarly, to convert an N-bit fraction to an integer, multiply the fractional value by  $2^{N-1}$ .



Figure 4-12: Different Representations of 0x4001

Figure 4-13: Different Representations of 0xC002



### 4.12 ACCUMULATOR USAGE (dsPIC30F, dsPIC33F AND dsPIC33E DEVICES)

Accumulators A and B are utilized by DSP instructions to perform mathematical and shifting operations. Since the accumulators are 40 bits wide and the X and Y data paths are only 16 bits, the method to load and store the accumulators must be understood.

Item A in Figure 4-14 shows that each 40-bit Accumulator (ACCA and ACCB) consists of an 8-bit Upper register (ACCxU), a 16-bit High register (ACCxH) and a 16-bit Low register (ACCxL). To address the bus alignment requirement and provide the ability for 1.31 math, ACCxH is used as a destination register for loading the accumulator (with the LAC instruction), and also as a source register for storing the accumulator (with the SAC. R instruction). This is represented by Item B, Figure 4-14, where the upper and lower portions of the accumulator are shaded. In reality, during accumulator loads, ACCxL is zero backfilled and ACCxU is sign-extended to represent the sign of the value loaded in ACCxH.

When Normal (31-bit) Saturation is enabled, DSP operations (such as ADD, MAC, MSC, etc.) utilize solely ACCxH:ACCxL (Item C in Figure 4-14) and ACCxU is only used to maintain the sign of the value stored in ACCxH:ACCxL. For instance, when a MPY instruction is executed, the result is stored in ACCxH:ACCxL, and the sign of the result is extended through ACCxU.

When Super Saturation is enabled, or when saturation is disabled, all registers of the accumulator may be used (Item D in Figure 4-14) and the results of DSP operations are stored in ACCxU:ACCxH:ACCxL. The benefit of ACCxU is that it increases the dynamic range of the accumulator, as described in **Section 4.11.1 "Integer and Fractional Data**". Refer to Table 4-10 to see the range of values which may be stored in the accumulator when in Normal and Super Saturation modes.



Figure 4-14: Accumulator Alignment and Usage

### 4.13 ACCUMULATOR ACCESS (dsPIC30F, dsPIC33F AND dsPIC33E DEVICES)

The six registers of Accumulator A and Accumulator B are memory mapped like any other Special Function Register. This feature allows them to be accessed with file register or indirect addressing, using any instruction which supports such addressing. However, it is recommended that the DSP instructions LAC, SAC and SAC. R be used to load and store the accumulators, since they provide sign-extension, shifting and rounding capabilities. LAC, SAC and SAC. R instruction details are provided in Section 5. "Instruction Descriptions".

- **Note 1:** For convenience, ACCAU and ACCBU are sign-extended to 16 bits. This provides the flexibility to access these registers using either Byte or Word mode (when file register or indirect addressing is used).
  - The OA, OB, SA or SB bit cannot be set by writing overflowed values to the memory mapped accumulators using MOV instructions, as these status bits are only affected by DSP operations.

### 4.14 DSP MAC INSTRUCTIONS (dsPIC30F, dsPIC33F AND dsPIC33E DEVICES)

The DSP Multiply and Accumulate (MAC) operations are a special suite of instructions which provide the most efficient use of the dsPIC30F, dsPIC33F, and dsPIC33E architectures. The DSP MAC instructions, shown in Table 4-11, utilize both the X and Y data paths of the CPU core, which enables these instructions to perform the following operations all in one cycle:

- two reads from data memory using prefetch working registers (MAC Prefetches)
- two updates to prefetch working registers (MAC Prefetch Register Updates)
- one mathematical operation with an accumulator (MAC Operations)

In addition, four of the ten DSP MAC instructions are also capable of performing an operation with one accumulator, while storing out the rounded contents of the alternate accumulator. This feature is called accumulator Write Back (WB) and it provides flexibility for the software developer. For instance, the accumulator WB may be used to run two algorithms concurrently, or efficiently process complex numbers, among other things.

Instruction	Description	Accumulator WB?
CLR	Clear accumulator	Yes
ED	Euclidean distance (no accumulate)	No
EDAC	Euclidean distance	No
MAC	Multiply and accumulate	Yes
MAC	Square and accumulate	No
MOVSAC	Move from X and Y bus	Yes
MPY	Multiply to accumulator	No
MPY	Square to accumulator	No
MPY.N	Negative multiply to accumulator	No
MSC	Multiply and subtract	Yes

### Table 4-11: DSP MAC Instructions

### 4.14.1 MAC Prefetches

Prefetches (or data reads) are made using the effective address stored in the working register. The two prefetches from data memory must be specified using the working register assignments shown in Table 4-9. One read must occur from the X data bus using W8 or W9, and one read must occur from the Y data bus using W10 or W11. The allowed destination registers for both prefetches are W4-W7.

As shown in Table 4-3, one special Addressing mode exists for the MAC class of instructions. This mode is the Register Offset Addressing mode and utilizes W12. In this mode, the prefetch is made using the effective address of the specified working register, plus the 16-bit signed value stored in W12. Register Offset Addressing may only be used in the X space with W9, and in the Y-space with W11.

### 4.14.2 MAC Prefetch Register Updates

After the MAC prefetches are made, the effective address stored in each prefetch working register may be modified. This feature enables efficient single-cycle processing for data stored sequentially in X and Y memory. Since all DSP instructions execute in Word mode, only even numbered updates may be made to the effective address stored in the working register. Allowable address modifications to each prefetch register are -6, -4, -2, 0 (no update), +2, +4 and +6. This means that effective address updates may be made up to 3 words in either direction.

When the Register Offset Addressing mode is used, no update is made to the base prefetch register (W9 or W11), or the offset register (W12).

### 4.14.3 MAC Operations

The mathematical operations performed by the MAC class of DSP instructions center around multiplying the contents of two working registers and either adding or storing the result to either Accumulator A or Accumulator B. This is the operation of the MAC, MPY, MPY.N and MSC instructions. Table 4-9 shows that W4-W7 must be used for data source operands in the MAC class of instructions. W4-W7 may be combined in any fashion, and when the same working register is specified for both operands, a square or square and accumulate operation is performed.

For the ED and EDAC instructions, the same multiplicand operand must be specified by the instruction, because this is the definition of the Euclidean Distance operation. Another unique feature about this instruction is that the values prefetched from X and Y memory are not actually stored in W4-W7. Instead, only the difference of the prefetched data words is stored in W4-W7.

The two remaining MAC class instructions, CLR and MOVSAC, are useful for initiating or completing a series of MAC or EDAC instructions and do not use the multiplier. CLR has the ability to clear Accumulator A or B, prefetch two values from data memory and store the contents of the other accumulator. Similarly, MOVSAC has the ability to prefetch two values from data memory and store the contents of either accumulator.

### 4.14.4 MAC Write Back

The write back ability of the MAC class of DSP instructions facilitates efficient processing of algorithms. This feature allows one mathematical operation to be performed with one accumulator, and the rounded contents of the other accumulator to be stored in the same cycle. As indicated in Table 4-9, register W13 is assigned for performing the write back, and two Addressing modes are supported: Direct and Indirect with Post-Increment.

The CLR, MOVSAC and MSC instructions support accumulator Write Back, while the ED, EDAC, MPY and MPY. N instructions do not support accumulator Write Back. The MAC instruction, which multiplies two working registers which are not the same, also supports accumulator Write Back. However, the square and accumulate MAC instruction does not support accumulator Write Back (see Table 4-11).

### 4.14.5 MAC Syntax

The syntax of the MAC class of instructions can have several formats, which depend on the instruction type and the operation it is performing, with respect to prefetches and accumulator Write Back. With the exception of the CLR and MOVSAC instructions, all MAC class instructions must specify a target accumulator along with two multiplicands, as shown in Example 4-19.

; MAC with no prefetch MAC W4*W5, A	
; MAC with no prefetch MAC W7*W7, B	
	→ Multiply W7*W7, Accumulate to ACCB

**instruction Set** 

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S

If a prefetch is used in the instruction, the assembler is capable of discriminating between the X or Y data prefetch based on the register used for the effective address. [W8] or [W9] specifies the X prefetch and [W10] or [W11] specifies the Y prefetch. Brackets around the working register are required in the syntax, and they designate that indirect addressing is used to perform the prefetch. When address modification is used, it must be specified using a minus-equals or plus-equals "C"-like syntax (i.e., "[W8] – = 2" or "[W8] + = 6"). When Register Offset Addressing is used for the prefetch, W12 is placed inside the brackets ([W9 + W12] for X prefetches and [W11 + W12] for Y prefetches). Each prefetch operation must also specify a prefetch destination register (W4-W7). In the instruction syntax, the destination register appears before the prefetch register. Legal forms of prefetch are shown in Example 4-20.





If an accumulator Write Back is used in the instruction, it is specified last. The Write Back must use the W13 register, and allowable forms for the Write Back are "W13" for direct addressing and "[W13] + = 2" for indirect addressing with post-increment. By definition, the accumulator not used in the mathematical operation is stored, so the Write Back accumulator is not specified in the instruction. Legal forms of accumulator Write Back (WB) are shown in Example 4-21.



Putting it all together, an MSC instruction which performs two prefetches and a write back is shown in Example 4-22.

### Example 4-22: MSC Instruction with Two Prefetches and Accumulator Write Back



4 Instruction Set Details

# 4.15 DSP ACCUMULATOR INSTRUCTIONS (dsPIC30F, dsPIC33F AND dsPIC33E DEVICES)

The DSP Accumulator instructions do not have prefetch or accumulator WB ability, but they do provide the ability to add, negate, shift, load and store the contents of either 40-bit Accumulator. In addition, the ADD and SUB instructions allow the two accumulators to be added or subtracted from each other. DSP Accumulator instructions are shown in Table 4-12 and instruction details are provided in Section 5. "Instruction Descriptions".

Instruction	Description	Accumulator WB?
ADD	Add accumulators	No
ADD	16-bit signed accumulator add	No
LAC	Load accumulator	No
NEG	Negate accumulator	No
SAC	Store accumulator	No
SAC.R	Store rounded accumulator	No
SFTAC	Arithmetic shift accumulator by Literal	No
SFTAC	Arithmetic shift accumulator by (Wn)	No
SUB	Subtract accumulators	No

Table 4-12: DSP Accumulator Instructions

# 4.16 SCALING DATA WITH THE FBCL INSTRUCTION (dsPIC30F, dsPIC33F AND dsPIC33E DEVICES)

To minimize quantization errors that are associated with data processing using DSP instructions, it is important to utilize the complete numerical result of the operations. This may require scaling data up to avoid underflow (i.e., when processing data from a 12-bit ADC), or scaling data down to avoid overflow (i.e., when sending data to a 10-bit DAC). The scaling, which must be performed to minimize quantization error, depends on the dynamic range of the input data which is operated on, and the required dynamic range of the output data. At times, these conditions may be known beforehand and fixed scaling may be employed. In other cases, scaling conditions may not be fixed or known, and then dynamic scaling must be used to process data.

The FBCL instruction (Find First Bit Change Left) can efficiently be used to perform dynamic scaling, because it determines the exponent of a value. A fixed point or integer value's exponent represents the amount which the value may be shifted before overflowing. This information is valuable, because it may be used to bring the data value to "full scale", meaning that its numeric representation utilizes all the bits of the register it is stored in.

The FBCL instruction determines the exponent of a word by detecting the first bit change starting from the value's sign bit and working towards the LSB. Since the dsPIC DSC device's barrel shifter uses negative values to specify a left shift, the FBCL instruction returns the negated exponent of a value. If the value is being scaled up, this allows the ensuing shift to be performed immediately with the value returned by FBCL. Additionally, since the FBCL instruction only operates on signed quantities, FBCL produces results in the range of -15:0. When the FBCL instruction returns '0', it indicates that the value is already at full scale. When the instruction returns -15, it indicates that the value cannot be scaled (as is the case with 0x0 and 0xFFFF). Table 4-13 shows word data with various dynamic ranges, their exponents, and the value after scaling each data to maximize the dynamic range. Example 4-23 shows how the FBCL instruction may be used for block processing.

Word Value	Exponent	Full Scale Value (Word Value << Exponent)
0x0001	14	0x4000
0x0002	13	0x4000
0x0004	12	0x4000
0x0100	6	0x4000
0x01FF	6	0x7FC0
0x0806	3	0x4030
0x2007	1	0x400E
0x4800	0	0x4800
0x7000	0	0x7000
0x8000	0	0x8000
0x900A	0	0x900A
0xE001	2	0x8004
0xFF07	7	0x8380

Table 4-13: Scaling Examples

Note: For the word values 0x0000 and 0xFFFF, the FBCL instruction returns -15.

As a practical example, assume that block processing is performed on a sequence of data with very low dynamic range stored in 1.15 fractional format. To minimize quantization errors, the data may be scaled up to prevent any quantization loss which may occur as it is processed. The FBCL instruction can be executed on the sample with the largest magnitude to determine the optimal scaling value for processing the data. Note that scaling the data up is performed by left shifting the data. This is demonstrated with the code snippet below.

#### Example 4-23: Scaling with FBCL

; assume W0 contains the largest absolute value of the data block			
; assume W4 points to the beginning of the data block			
; assume the block of data contains BLOCK SIZE words			
; determine the exponent to use for scaling			
FBCL W0, W2 ; store exponent in W2			
; scale the entire data block before processing			
D0 #(BLOCK_SIZE-1), SCALE			
LAC [W4], A ; move the next data sample to ACCA			
SFTAC A, W2 ; shift ACCA by W2 bits			
SCALE:			
SAC A, [W4++] ; store scaled input (overwrite original)			
; now process the data			
; (processing block goes here)			
, (processing brock goes nere)			

## 4.17 NORMALIZING THE ACCUMULATOR WITH THE FBCL INSTRUCTION (dsPIC30F, dsPIC33F AND dsPIC33E DEVICES)

The process of scaling a quantized value for its maximum dynamic range is known as normalization (the data in the third column in Table 4-13 contains normalized data). Accumulator normalization is a technique used to ensure that the accumulator is properly aligned before storing data from the accumulator, and the FBCL instruction facilitates this function.

The two 40-bit accumulators each have 8 guard bits from the ACCxU register, which expands the dynamic range of the accumulators from 1.31 to 9.31, when operating in Super Saturation mode (see Section 4.11.1 "Integer and Fractional Data"). However, even in Super Saturation mode, the Store Rounded Accumulator (SAC.R) instruction only stores 16-bit data (in 1.15 format) from ACCxH, as described in Section 4.12 "Accumulator Usage (dsPIC30F, dsPIC33F and dsPIC33E Devices)". Under certain conditions, this may pose a problem.

Proper data alignment for storing the contents of the accumulator may be achieved by scaling the accumulator down if ACCxU is in use, or scaling the accumulator up if all of the ACCxH bits are not being used. To perform such scaling, the FBCL instruction must operate on the ACCxU byte and it must operate on the ACCxH word. If a shift is required, the ALU's 40-bit shifter is employed, using the SFTAC instruction to perform the scaling. Example 4-24 contains a code snippet for accumulator normalization.

### Example 4-24: Normalizing with FBCL

; assume a	n operation in A	CCA has just completed (SR intact)	
; assume tl	he processor is :	in super saturation mode	
; assume A	CCAH is defined	to be the address of ACCAH (0x24)	
MOV	#ACCAH, W5	; W5 points to ACCAH	
BRA	OA, FBCL_GUARD	; if overflow we right shift	
FBCL_HI:			
FBCL	[W5], W0	; extract exponent for left shift	
BRA	SHIFT_ACC	; branch to the shift	
FBCL_GUARD	:		
FBCL	[++W5], W0	; extract exponent for right shift	
ADD.B	W0, #15, W0	; adjust the sign for right shift	
SHIFT_ACC:			
SFTAC	A, W0	; shift ACCA to normalize	

# 4.18 EXTENDED-PRECISON ARITHMETIC USING MIXED-SIGN MULTIPLICATIONS (dsPIC33E ONLY)

Many DSP algorithms utilize extended-precision arithmetic operations (operations with 32-bit or 64-bit operands and results) to enhance the resolution and accuracy of computations. These can be implemented using 16-bit signed or unsigned multiplications; however, this would require some additional processing and shifting of the data to obtain the correct results. To enable such extended-precision algorithms to be computed faster, dsPIC33E devices support an optional implicit mixed-sign multiplication mode, which is selected by setting US<1:0> (CORCON<13:12>) = '10'.

In this mode, mixed-sign (unsigned x signed and signed x unsigned) multiplications can be performed without the need to dynamically reconfigure the US<1:0> bits and shift data to account for the difference in operand formats. Moreover, signed x signed and unsigned x unsigned multiplications can also be performed without changing the multiplication mode. Each input operand is implicitly treated as an unsigned number if the working register being used to specify the operand is either W4 or W6. Similarly, an operand is treated as a signed number if the register used is either W5 or W7. The DSP Engine selects the type of multiplication to be performed based on the operand registers used, thereby eliminating the need for the user software to modify the US<1:0> bits.

The execution time reductions provided by the implicit mixed-sign multiplication feature is illustrated in the following code example, where the instruction cycle count for performing a 32-bit multiplication is reduced from 7 cycles to 4 cycles when the mixed-sign multiplication mode is enabled.

Example 4-25:	32-bit Signed Multi	plication using Im	plicit Mixed-Sign Mode

<pre>Case A - Mixed-Sign Multiplication Mode Not Enabled MUL.SU W5, W6, W0; Word1 (signed) x Word2 (unsigned) MUL.US W4, W7, W2; Word0 (unsigned) x Word3 (signed) CLR B ; Clear Accumulator B ADD W1, B ADD W3, B SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format MAC W5*W7, B; Word1 (signed) x Word 3 (signed) Case B - Mixed-Sign Multiplication Mode Enabled MPY W5*W6, B; Word1 (signed) x Word2 (unsigned) MAC W4*W7, B; Word0 (unsigned) x Word3 (signed) SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format MAC W5*W7, B; Word1 (signed) x Word3 (signed)</pre>		
<pre>MUL.US W4, W7, W2; Word0 (unsigned) x Word3 (signed) CLR B ; Clear Accumulator B ADD W1, B ADD W3, B SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format MAC W5*W7, B; Word1 (signed) x Word 3 (signed) Case B - Mixed-Sign Multiplication Mode Enabled MPY W5*W6, B; Word1 (signed) x Word2 (unsigned) MAC W4*W7, B; Word0 (unsigned) x Word3 (signed) SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format</pre>	Case A	- Mixed-Sign Multiplication Mode Not Enabled
<pre>ADD W1, B ADD W3, B SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format MAC W5*W7, B; Word1 (signed) x Word 3 (signed) Case B - Mixed-Sign Multiplication Mode Enabled MPY W5*W6, B; Word1 (signed) x Word2 (unsigned) MAC W4*W7, B; Word0 (unsigned) x Word3 (signed) SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format</pre>		
<ul> <li>ADD W3, B</li> <li>SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format</li> <li>MAC W5*W7, B; Word1 (signed) x Word 3 (signed)</li> <li><b>Case B</b> - Mixed-Sign Multiplication Mode Enabled</li> <li>MPY W5*W6, B; Word1 (signed) x Word2 (unsigned)</li> <li>MAC W4*W7, B; Word0 (unsigned) x Word3 (signed)</li> <li>SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format</li> </ul>	CLR	B ; Clear Accumulator B
<pre>SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format MAC W5*W7, B; Word1 (signed) x Word 3 (signed) Case B - Mixed-Sign Multiplication Mode Enabled MPY W5*W6, B; Word1 (signed) x Word2 (unsigned) MAC W4*W7, B; Word0 (unsigned) x Word3 (signed) SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format</pre>	ADD	W1, B
<ul> <li>MAC W5*W7, B; Word1 (signed) x Word 3 (signed)</li> <li>Case B - Mixed-Sign Multiplication Mode Enabled</li> <li>MPY W5*W6, B; Word1 (signed) x Word2 (unsigned)</li> <li>MAC W4*W7, B; Word0 (unsigned) x Word3 (signed)</li> <li>SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format</li> </ul>	ADD	WЗ, В
MPY W5*W6, B; Word1 (signed) x Word2 (unsigned) MAC W4*W7, B; Word0 (unsigned) x Word3 (signed) SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format		
MAC W4*W7, B; Word0 (unsigned) x Word3 (signed) SFTAC B, #15 ; Shift right by 15 bits to align for Q31 format	Case B	- Mixed-Sign Multiplication Mode Enabled
	MAC SFTAC	W4*W7, B; Word0 (unsigned) x Word3 (signed) B, #15 ; Shift right by 15 bits to align for Q31 format

Besides DSP instructions, MCU multiplication (MUL) instructions can also utilize Accumulator A or Accumulator B as a result destination, which enables faster extended-precision arithmetic even when not using DSP multiplication instructions such as MPY or MAC.



## **Section 5. Instruction Descriptions**

### HIGHLIGHTS

This section of the manual contains the following major topics:

5.1	Instruction Symbols	94
5.2	Instruction Encoding Field Descriptors Introduction	94
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Descriptions

### 5.1 INSTRUCTION SYMBOLS

All the symbols used in **Section 5.4 "Instruction Descriptions"** are listed in Table 1-2.

### 5.2 INSTRUCTION ENCODING FIELD DESCRIPTORS INTRODUCTION

All instruction encoding field descriptors used in **Section 5.4 "Instruction Descriptions"** are shown in Table 5-2 through Table 5-12.

Table 5-1: Instruction Encoding Field Descriptors

Field	Description
A <sup>(1)</sup>	Accumulator selection bit: 0 = ACCA; 1 = CCB
aa <sup>(1)</sup>	Accumulator Write Back mode (see Table 5-12)
B	Byte mode selection bit: $0 =$ word operation; $1 =$ byte operation
bbbb	4-bit bit position select: 0000 = LSB; 1111 = MSB
D	Destination address bit: 0 = result stored in WREG;
	1 = result stored in file register
dddd	Wd destination register select: 0000 = W0; 1111 = W15
f ffff ffff ffff	13-bit register file address (0x0000 to 0x1FFF)
fff ffff ffff ffff	15-bit register file word address (implied 0 LSB) (0x0000 to 0xFFFE)
ffff ffff ffff ffff	16-bit register file byte address (0x0000 to 0xFFFF)
<u>ggg</u>	Register Offset Addressing mode for Ws source register (see Table 5-4)
hhh	Register Offset Addressing mode for Wd destination register (see Table 5-5)
<sub>iiii</sub> (1)	Prefetch X Operation (see Table 5-6)
jjjj <b>(1)</b>	Prefetch Y Operation (see Table 5-8)
k	1-bit literal field, constant data or expression
kkkk	4-bit literal field, constant data or expression
kk kkkk	6-bit literal field, constant data or expression
kkkk kkkk	8-bit literal field, constant data or expression
kk kkkk kkkk	10-bit literal field, constant data or expression
kk kkkk kkkk kkkk	14-bit literal field, constant data or expression
kkkk kkkk kkkk kkkk	16-bit literal field, constant data or expression
mm	Multiplier source select with same working registers (see Table 5-10)
mmm	Multiplier source select with different working registers (see Table 5-11)
nnnn nnnn nnnn nnn0	23-bit program address for CALL and GOTO instructions
nnn nnnn	
nnnn nnnn nnnn nnnn	16-bit program offset field for relative branch/call instructions
ррр	Addressing mode for Ws source register (see Table 5-2)
qqq	Addressing mode for Wd destination register (see Table 5-3)
rrrr	Barrel shift count
SSSS	Ws source register select: 0000 = W0; 1111 = W15
tttt	Dividend select, most significant word
VVVV	Dividend select, least significant word
W	Double Word mode selection bit: 0 = word operation; 1 = double word operation
WWWW	Wb base register select: 0000 = W0; 1111 = W15
<sub>XX</sub> (1)	Prefetch X Destination (see Table 5-7)
XXXX XXXX XXXX XXXX	16-bit unused field (don't care)
yy <sup>(1)</sup>	Prefetch Y Destination (see Table 5-9)
Z	Bit test destination: $0 = C$ flag bit; $1 = Z$ flag bit

**Note 1:** This field is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.

ррр	Addressing Mode	Source Operand
000	Register Direct	Ws
001	Indirect	[Ws]
010	Indirect with Post-Decrement	[Ws]
011	Indirect with Post-Increment	[Ws++]
100	Indirect with Pre-Decrement	[Ws]
101	Indirect with Pre-Increment	[++Ws]
11x	Unused	

Table 5-2:Addressing Modes for Ws Source Register

### Table 5-3: Addressing Modes for Wd Destination Register

qqq	Addressing Mode	Destination Operand
000	Register Direct	Wd
001	Indirect	[Wd]
010	Indirect with Post-Decrement	[Wd]
011	Indirect with Post-Increment	[Wd++]
100	Indirect with Pre-Decrement	[Wd]
101	Indirect with Pre-Increment	[++Wd]
11x	Unused (an attempt to use this Addressing mode will force a RESET instruction)	

### Table 5-4: Offset Addressing Modes for Ws Source Register (with Register Offset)

ggg	Addressing Mode	Source Operand
000	Register Direct	Ws
001	Indirect	[Ws]
010	Indirect with Post-Decrement	[Ws]
011	Indirect with Post-Increment	[Ws++]
100	Indirect with Pre-Decrement	[Ws]
101	Indirect with Pre-Increment	[++Ws]
11x	Indirect with Register Offset	[Ws+Wb]

### Table 5-5: Offset Addressing Modes for Wd Destination Register (with Register Offset)

hhh	Addressing Mode	Source Operand
000	Register Direct	Wd
001	Indirect	[Wd]
010	Indirect with Post-Decrement	[Wd]
011	Indirect with Post-Increment	[Wd++]
100	Indirect with Pre-Decrement	[Wd]
101	Indirect with Pre-Increment	[++Wd]
11x	Indirect with Register Offset	[Wd+Wb]

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iiii	Operation	
0000	Wxd = [W8]	
0001	Wxd = [W8], W8 = W8 + 2	
0010	Wxd = [W8], W8 = W8 + 4	
0011	Wxd = [W8], W8 = W8 + 6	
0100	No Prefetch for X Data Space	
0101	Wxd = [W8], W8 = W8 – 6	
0110	Wxd = [W8], W8 = W8 – 4	
0111	Wxd = [W8], W8 = W8 – 2	
1000	Wxd = [W9]	
1001	Wxd = [W9], W9 = W9 + 2	
1010	Wxd = [W9], W9 = W9 + 4	
1011	Wxd = [W9], W9 = W9 + 6	
1100	Wxd = [W9 + W12]	
1101	Wxd = [W9], W9 = W9 - 6	
1110	Wxd = [W9], W9 = W9 – 4	
1111	Wxd = [W9], W9 = W9 – 2	

### Table 5-6: X Data Space Prefetch Operation (dsPIC30F, dsPIC33F and dsPIC33E)

### Table 5-7: X Data Space Prefetch Destination (dsPIC30F, dsPIC33F and dsPIC33E)

хх	Wxd
00	W4
01	W5
10	W6
11	W7

### Table 5-8: Y Data Space Prefetch Operation (dsPIC30F, dsPIC33F and dsPIC33E)

jjjj	Operation
0000	Wyd = [W10]
0001	Wyd = [W10], W10 = W10 + 2
0010	Wyd = [W10], W10 = W10 + 4
0011	Wyd = [W10], W10 = W10 + 6
0100	No Prefetch for Y Data Space
0101	Wyd = [W10], W10 = W10 - 6
0110	Wyd = [W10], W10 = W10 - 4
0111	Wyd = [W10], W10 = W10 - 2
1000	Wyd = [W11]
1001	Wyd = [W11], W11 = W11 + 2
1010	Wyd = [W11], W11 = W11 + 4
1011	Wyd = [W11], W11 = W11 + 6
1100	Wyd = [W11 + W12]
1101	Wyd = [W11], W11 = W11 - 6
1110	Wyd = [W11], W11 = W11 - 4
1111	Wyd = [W11], W11 = W11 - 2

### Table 5-9: Y Data Space Prefetch Destination (dsPIC30F, dsPIC33F and dsPIC33E)

уу	Wyd
00	W4
01	W5
10	W6
11	W7

### Table 5-10: MAC or MPY Source Operands (Same Working Register) (dsPIC30F, dsPIC33F and dsPIC33E)

mm	Multiplicands
00	W4 * W4
01	W5 * W5
10	W6 * W6
11	W7 * W7

### Table 5-11: MAC or MPY Source Operands (Different Working Register) (dsPIC30F, dsPIC33F and dsPIC33E)

mmm	Multiplicands
000	W4 * W5
001	W4 * W6
010	W4 * W7
011	Invalid
100	W5 * W6
101	W5 * W7
110	W6 * W7
111	Invalid

### Table 5-12: MAC Accumulator Write Back Selection (dsPIC30F, dsPIC33F and dsPIC33E)

aa	Write Back Selection
00	W13 = Other Accumulator (Direct Addressing)
01	[W13] + = 2 = Other Accumulator (Indirect Addressing with Post-Increment)
10	No Write Back
11	Invalid

### Table 5-13: MOVPAG Destination Selection

PP	Target Page Register					
00	DSRPAG					
01	DSWPAG					
10	TBLPAG					
11	Reserved – do not use					

### Table 5-14: Accumulator Selection

Α	Target Accumulator
0	Accumulator A
1	Accumulator B

### 5.3 INSTRUCTION DESCRIPTION EXAMPLE

The example description below is for the fictitious instruction F00. The following example instruction was created to demonstrate how the table fields (syntax, operands, operation, etc.) are used to describe the instructions presented in **Section 5.4 "Instruction Descriptions"**.

FOO	The Header field summarizes what the instruction does							
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
				Х	Х	Х		
	Cells marked with an 'X' indicate the instruction is implemented for that device family.							
Syntax:	The Syntax field consists of an optional label, the instruction mnemonic, optional extensions which exist for the instruction and the operands for instruction. Most instructions support more than one operand variant to support the various Addressing modes. In these circumstances, all pos- instruction operands are listed beneath each other and are enclosed in braces.							
Operands:	may take. C	nds field desc Operands may signed or uns	/ be accumula	ator registers	, file registers			
Operation:	The Operat	ion field sumr	marizes the o	peration perfo	ormed by the	instruction.		
Status Affected:		Affected field the instruction order.						
Encoding: The Encoding field shows how the instruction is a fields are explained in the Description field, and c are provided in Table 5.2.								
Description: The Description field describes in detail the operation performance instruction. A key for the encoding bits is also provided.					by the			
Words:	The Words field contains the number of program words that are used to store the instruction in memory.							
Cycles:	The Cycles field contains the number of instruction cycles that are required to execute the instruction.							
Examples:	The Examples field contains examples that demonstrate how the instructi operates. "Before" and "After" register snapshots are provided, which allo the user to clearly understand what operation the instruction performs.							

### 5.4 INSTRUCTION DESCRIPTIONS

ADD	Add f to WREG					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	ADD{.B}	f	{,WREG}		
-	f ∈ [0 81	. ,		(,		
Operation:	-	G) →destinati	ion designate	ed by D		
Status Affected:	DC, N, OV,		- U			
Encoding:	1011	0100	0BDf	ffff	ffff	ffff
	specified, th result is sto The 'B' bit s The 'D' bit s	REG operand he result is sto ored in the file selects byte o selects the de select the ado	ored in WRE register. or word opera estination ('0'	G. If WREG i ation ('0' for w ' for WREG, '2	s not specifie	ed, the yte).
	1	The extensior rather than a denote a word The WREG is	word operati d operation, l	on. You may but it is not re	use a .W ext equired.	-
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-mod details, se <u>Example 1:</u> AC WREC	ify-write ope ee <b>Note 3</b> in DD.B Before Instruction G CC80	WR	n-CPU Speci <b>1 "Multi-Cyc</b> ; Add N After Instruction EG CC80	ial Function R l <b>e Instructio</b> n WREG to RAM	Registers. For ns".	more
RAM10 SF		RAM:	100 FF40 SR 0005	(OV, C = 1)		

ADD	Add Literal to Wn							
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	ADD{.B}	#lit10,	Wn				
Operands:	lit10 $\in$ [0 255] for byte operation lit10 $\in$ [0 1023] for word operation Wn $\in$ [W0 W15]							
Operation:	lit10 + (Wn)	) →Wn						
Status Affected:	DC, N, OV,	Z, C						
Encoding:	1011	0000	0Bkk	kkkk	kkkk	dddd		
Description:		-bit unsigned l n, and place th						
	The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'k' bits specify the literal operand. The 'd' bits select the address of the working register.							
	2:	rather than a v denote a worc For byte opera value [0:255]. for informatior	l operation, b ations, the lite See <mark>Section</mark>	ut it is not rec eral must be s <b>4.6 "Using 1</b>	luired. pecified as a <mark>0-bit Literal (</mark>	n unsigned <b>Dperands"</b>		
Words:	1							
Cycles:	1							
Example 1:	ADD.B	#0xFF, W7	; Add	-1 to W7 (	Byte mode)			
	Before Instructio W7 12C0 SR 0000	on )	After Instructio W7 12BF SR 0009					
Example 2:	ADD	#0xFF, W1	; Add	255 to W1	(Word mode)			
	Before Instructio W1 12C0 SR 0000	on )	After Instructio W1 13BF SR 0000	-				

ADD		Add Wb to	Short Litera	d				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	ADD{.B}	Wb,	#lit5,	Wd [Wd]			
					[Wd++]			
					[Wd]			
					[++Wd]			
					[Wd]			
Operands:	Wb ∈ [W0 lit5 ∈ [0 Wd ∈ [W0	31]						
Operation:	(Wb) + lit5	→Wd						
Status Affected:	DC, N, OV	/, Z, C						
Encoding:	0100	0www	wBqq	qddd	d11k	kkkk		
Description:	Add the contents of the base register Wb to the 5-bit unsigned short literal operand, and place the result in the destination register Wd. Register direct addressing must be used for Wb. Either register direct or indirect addressing may be used for Wd.							
	The 'w' bits select the address of the base register. The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'q' bits select the destination Address mode. The 'd' bits select the destination register. The 'k' bits provide the literal operand, a five-bit integer number.							
	Note:	rather than a	word opera	instruction d tion. You ma but it is not r	yuse a .We			
Words:	1		-					
Cycles:	1							
Example 1:	ADD.B	W0, #0x1F,		Add W0 and Store the r				
	Before Instructio W0 2290	n 1	After Instructio	on T				

Example 2: AI	DD	W3, #0x6, [			6 (Word mod esult in [	•
W W Data 0FF Data 100 SI	4 1000 E DDEE 0 DDEE			n       		
ADD		Add Wb to V	Ns			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	ADD{.B}	Wb,	Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws],	Wd [Wd] [Wd++] [Wd] [++Wd] [Wd]	
Operands:	Wb ∈ [W0 Ws ∈ [W0 Wd ∈ [W0	W15]				
Operation:	(Wb) + (W	s) →Wd				
Status Affected:	DC, N, OV	, Z, C				
Encoding:	0100	0www	wBqq	qddd	dppp	SSSS
Description:	Add the contents of the source register Ws and the contents of the base register Wb, and place the result in the destination register Wd. Register direct addressing must be used for Wb. Either register direct or indirect addressing may be used for Ws and Wd. The 'w' bits select the address of the base register. The 'B' bit selects byte or word operation ('0' for word, '1' for byte).					
	The 'q' bits select the destination Address mode. The 'd' bits select the destination register. The 'p' bits select the source Address mode. The 's' bits select the source register.					
	Note:	The extension rathjer than a denote a wor	a word opera	tion. You ma	y use a .We	•
Words:	1					
Cycles:	1 <sup>(1)</sup>					
Note 1: In dsPIC3	33E and PIC	24E devices,	the listed cyc	le count doe	s not apply to	read and

**Note 1:** In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see **Note 3** in **Section 3.2.1** "Multi-Cycle Instructions".

Example 1:	ADD.B V	15, W6,	W7		W5 to W6, te mode)	store resu	lt in W7
	Before Instruction W5 AB00 W6 0030 W7 FFFF SR 0000		W! W SF	6 0030 7 FF30			
Example 2:	ADD N	√5, W6,	W7		W5 to W6, rd mode)	store resul	lt in W7
	Before Instruction W5 AB00 W6 0030 W7 FFFF SR 0000		W5 W6 W7 SR	0030 AB30	l = 1)		
ADD				ulators			
Implemented in:	PIC24F	PIC	24H	PIC24E	dsPIC30F X	dsPIC33F X	dsPIC33E X
Syntax: Operands: Operation:	{label:} Acc ∈ [A,I <u>If (Acc = A</u> (ACCA) -	<u>):</u>	8) →A(	Acc			
Status Affected:	<u>Else:</u> (ACCA) - OA, OB, C	•			1	1	
Encoding: Description:		result in	of Accu		0000 the contents nulator. This		
Words: Cycles:	The 'A' bit 1 1	specifie	s the d	destination ad	ccumulator.		
Example 1:	ADD	A		; Add A	CCB to ACCA		
				ACCA ACCB SR	After Instructio 00 1855 7 00 1833 4 0	858	

5

Example 2:	ADD	В	; Assume	•	ration mode = 1, SATB		
	Instr CCA 00 E	fore uction 111 2222 554 3210 0000	ACCA ACCB SR	After Instruction 00 E111 22 01 5765 54 48	22	B = 1)	
ADD		16-bit Signe	d Add to Acc	umulator			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
				Х	Х	Х	
Syntax:	{label:}	ADD	Ws, [Ws], [Ws++], [Ws], [Ws], [++Ws], [Ws+Wb],	{#Slit4,}	Acc		
Operands:	$\label{eq:WS} \begin{array}{l} WS \in \left[WO \; . \right. \\ Wb \in \left[WO \; . \right. \\ Slit4 \in \left[ -8 \; \right. \\ Acc \in \left[ A, B \right] \end{array}$	W15] +7]					
Operation:	Shift <sub>Slit4</sub> (Ex	tend(Ws)) + (A	Acc) →Acc				
Status Affected:	OA, OB, OA	AB, SA, SB, SA	٩B				
Encoding:	1100	1001	Awww	wrrr	rggg	SSSS	
Description:	Add a 16-bit value specified by the source working register to the most significant word of the selected accumulator. The source operand may specify the direct contents of a working register or an effective address. The value specified is added to the most significant word of the accumulator by sign-extending and zero backfilling the source operand prior to the operation. The value added to the accumulator may also be shifted by a 4-bit signed literal before the addition is made.						
	The 'w' bits The 'r' bits The 'g' bits	pecifies the de specify the off encode the op select the sou specify the sou	set register W tional shift. rce Address n	/b. node.			
	i	Positive values and negative v left. The conte	alues of oper	and Slit4 rep	oresent an ari	thmetic shift	

ADD		16-bit Sig	gned Add to Acc	cumulator	
Words:	1				
Cycles:	1 <sup>(1)</sup>				
	read-modi	3E and PIC24E de fy-write operations e <b>Note 3</b> in <mark>Sectio</mark>	on non-CPU Spe	cial Function Regi	sters. For more
Example 1	<u>:</u> ADD	W0, #2, A	; Add W0 r	ight-shifted by	2 to ACCA
		Before		After	
		Instruction	1	Instruction	-
	W0		W		
	ACCA		ACCA		
	SR	0000	SF	R 0000	)
Example 2	: ADD	[W5++], A	; Add the e ; Post-incr	ffective value ement W5	of W5 to ACCA
		Before		After	
		Instruction		Instruction	_
	W5	2000	W5	2002	
	ACCA	00 0067 2345	ACCA	00 5067 2345	

Data 2000

SR

5000

0000

5000

0000

Data 2000

SR

5

ADDC		Add f to W	REG with C	arry		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	ADDC{.B}	f	{,WREG}		
Operands:	f∈ [0 81	91]				
Operation:	(f) + (WRE	G) + (C) →de	estination de	signated by I	C	
Status Affected:	DC, N, OV,	Z, C				
Encoding:	1011	0100	1BDf	ffff	ffff	ffff
	register. Th register. If V not specifie The 'B' bit : The 'D' bit	ster and the ne optional W WREG is spe- ed, the result selects byte of selects the do select the ad	REG operar ecified, the re is stored in t or word oper estination ('G	d determine sult is stored he file regist ation ('0' for ' for WREG,	s the destina d in WREG. I er. word, '1' for	ition f WREG is byte).
	2: 3:	The extensio rather than a denote a wor The WREG is The Z flag is instructions o	word operation, d operation, s set to work "sticky" for A	ion. You may but it is not i ing register \ .DDC, CPB, S	y use a .We required. W0.	xtension to
Words:	1					
Cycles:	1(1)					
read-moo details, s	lify-write ope ee <b>Note 3</b> in	24E devices, rations on no Section 3.2. AM100	n-CPU Spec 1 "Multi-Cyc	ial Function F I <b>e Instructio</b> /REG and C	Registers. Fo ons".	or more
WREC RAM10 SF Example 2: AD	0 8006 R 0001 (	RAM1	SR 0000	N RAM200 and	C bit to t	he WPEC
WREC	Before Instruction	WRI	; (Word After Instruction	l mode)		
RAM200 SF		RAM2 C=1) \$	00 3400 SR 000C	(N, OV = 1)		

ADDC		1	to Wn with	-	1				
Implemented in:		PIC24H	PIC24E	dsPIC30F	dsPIC33F				
	X	Х	Х	X	Х	Х			
Syntax:	{label:}	ADDC{.B}	#lit10,	Wn					
Operands:	lit10 ∈ [0	lit10 $\in$ [0 255] for byte operation lit10 $\in$ [0 1023] for word operation Wn $\in$ [W0 W15]							
Operation:	lit10 + (Wn	ı) + (C) →Wn							
Status Affected:	DC, N, OV,	, Z, C							
Encoding:	1011	0000	1Bkk	kkkk	kkkk	dddd			
Description:		)-bit unsigned I n and the Carr n.							
	The 'k' bits	The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'k' bits specify the literal operand. The 'd' bits select the address of the working register.							
	1	The extension rather than a v denote a word	word operati d operation, I	ion. You may but it is not re	use a .W ext equired.	tension to			
	2:	For byte operation operation operands for byte operation operands for byte mode.	rations, the lit ue [0:255]. Se	teral must be ee <mark>Section 4.</mark>	specified as .6 "Using 10	)-bit Literal			
	3:	The Z flag is " These instruct			SUBB and SI	UBBR.			
Words:	1								
Cycles:	1								
Example 1:	ADDC.B #0	0xFF, W7	; Add -1	and C bit 1	to W7 (Byte	mode)			
	Before Instruction		After Instruction						
	W7 12C0 SR 0000 (C	W7 C = 0) SF		N,C = 1)					
Example 2:	ADDC #0	0xFF, W1	; Add 25	5 and C bit	to W1 (Wor	rd mode)			
	Before Instruction W1 12C0 SR 0001 (C	W1 C = 1) SR							

ADDC		Add Wb to S	Short Literal	with Carry		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	ADDC{.B}	Wb,	#lit5,	Wd [Wd] [Wd++] [Wd] [++Wd] [Wd]	
Operands:	Wb ∈ [W0 lit5 ∈ [0 Wd ∈ [W0	31]				
Operation:	(Wb) + lit5	+ (C) →Wd				
Status Affected:	DC, N, OV	ν, Ζ, C				
Encoding:	0100	1www	wBqq	qddd	d11k	kkkk
	Wd. Regis indirect ad The 'W' bit The 'B' bit The 'q' bits The 'd' bits	nd the Carry b ter direct addre dressing may s select the ad selects byte of s select the des s select the des s provide the lit	essing must I be used for V dress of the I r word operat stination Add stination regis	be used for W Vd. base register. bion ('0' for wo ress mode. ster.	/b. Register c	lirect or te).
	Note 1: 2:	The extension rather than a v denote a word The Z flag is " instructions ca	word operatic d operation, b sticky" for AD	on. You may u out it is not rea DC, CPB, SL	use a . W exte quired.	nsion to
Words:	1					
Cycles:	1					
Example 1:	ADDC.B	W0, #0x1F,		d WO, 31 ar ore the res		
Data 1	Before           Instruction           W0         CC80           W7         12C0           2C0         B000           SR         0000	Data	Afte Instruc W0 CC W7 120 a 12C0 B00 SR 00	ction 80 C0		
Example 2: AI	DC	W3, #0>	<6, [W4]	; Add W3, 6 and C bit (Word mode) ; Store the result in [W4]		
---------------	------------	---------	-----------	---		
	Before			After		
	Instructio	n		Instruction		
W	6006	]	W3	6006		
W	4 1000		W4	OFFE		
Data 0FF	DDEE		Data 0FFE	600D		
Data 100	DDEE		Data 1000	DDEE		
SI	R 0001	(C = 1)	SR	0000		

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ADDC		Add Wb to	Ws with Car	ry				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	ADDC{.B}	Wb,	Ws,	Wd			
-	. ,			[Ws],	[Wd]			
				[Ws++],	[Wd++]			
				[Ws],	[Wd]			
				[++Ws],	[++Wd]			
				[Ws],	[Wd]			
Operands:	Wb ∈ [W0 Ws ∈ [W0 Wd ∈ [W0	W15]						
Operation:	(Wb) + (W	s) + (C) →Wd						
Status Affected:	DC, N, OV	, Z, C						
Encoding:	0100	1www	wBqq	qddd	dppp	SSSS		
Description:	Add the contents of the source register Ws, the contents of the base register Wb and the Carry bit, and place the result in the destination register Wd. Register direct addressing must be used for Wb. Either register direct or indirect addressing may be used for Ws and Wd.							
	The 'B' bit The 'q' bits The 'd' bits The 'p' bits	s select the ac selects byte c select the de select the de select the so select the so	r word opera stination Add stination regi urce Address	tion ('0' for w Iress mode. ster. 5 mode.		yte).		
	<b>Note 1:</b> The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a . W extension to denote a word operation, but it is not required.							
	2:	The Z flag is ' instructions c			JBB and SUE	BR. These		
Words:	1							
Cycles:	1 <sup>(1)</sup>							

read-modify-write operations on non-CPU Special Function Registers. For more details, see **Note 3** in **Section 3.2.1 "Multi-Cycle Instructions"**.

I	Before nstructio	n l	After nstruction
W0	CC20	W0	CC20
W1	0800	W1	0801
W2	1000	W2	1001
Data 0800	AB25	Data 0800	AB25
Data 1000	FFFF	Data 1000	FF46
SR	0001	(C = 1) SR	0000

W3,[W2++],[W1++]

Example 2: ADDC

; Add W3, [W2] and C bit (Word mode) ; Store the result in [W1] ; Post-increment W1, W2

	Before	-	After
I	nstructio	n I	nstruction
W1	1000	W1	1002
W2	2000	W2	2002
W3	0180	W3	0180
Data 1000	8000	Data 1000	2681
Data 2000	2500	Data 2000	2500
SR	0001	(C = 1) SR	0000

AND		AND f and V	WREG					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	AND{.B}	f	{,WREG}				
Operands:	f∈ [0 81	91]						
Operation:	(f).AND.(W	REG) →desti	nation desig	nated by D				
Status Affected:	N, Z							
Encoding:	1011	0110	0BDf	ffff	ffff	ffff		
	the destination destination If WREG is	REG and the option register. register. If W not specified	The optional REG is spec I, the result is	WREG operation operation with the results stored in the results stored in the results stored in the	and determin ult is stored ir e file register.	es the 1 WREG.		
	The 'D' bit s	selects byte o selects the de select the ado	estination ('0'	for WREG, "				
	<b>Note 1:</b> The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a . W extension to denote a word operation, but it is not required.							
	2:	The WREG is	s set to worki	ng register W	/0.			
Words:	1							
Cycles:	1 <sup>(1)</sup>							
read-m details,	C33E and PIC odify-write ope see <b>Note 3</b> in	erations on no Section 3.2.	on-CPU Spec 1 "Multi-Cyc	ial Function F le Instructio	Registers. For ns".	more		
Example 1:	AND.B RAM10	0	; AND W	REG to RAM1	loo (Bàte w	ode)		
WRE RAM1 S		WRI RAM1	.00 FF80	(N = 1)				
Example 2:	AND RAM200,	WREG	; AND R	AM200 to W	REG (Word m	ode)		
	Before Instruction		After Instructior	1				

	Before		After
I	nstructior	n Ir	nstructio
WREG	CC80	WREG	0080
RAM200	12C0	RAM200	12C0
SR	0000	SR	0000

AND		AND Litera	l and Wn						
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	AND{.B}	#lit10,	Wn					
Operands:	lit10 ∈ [0	lit10 $\in$ [0 255] for byte operation lit10 $\in$ [0 1023] for word operation Wn $\in$ [W0 W15]							
Operation:	lit10.AND.(	lit10.AND.(Wn) $\rightarrow$ Wn							
Status Affected:	N, Z								
Encoding:	1011	0010	0Bkk	kkkk	kkkk	dddd			
Description:	contents of	the working	D operation of register Wn a gister direct a	nd place the	result back i	nto the			
	The 'k' bits	specify the life	er word operat eral operand. dress of the v		-	/te).			
		<b>Note 1:</b> The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a .W extension to denote a word operation, but it is not required.							
	2:								
Words:	1								
Cycles:	1								
Example 1:	AND.B #0x83	8, W7	; AND 0>	<83 to W7 (	Byte mode)				
	Before Instruction W7 12C0 SR 0000		After Instruction W7 1280 SR 0008	(N = 1)					
Example 2:	AND #0x333,	W1	; AND 0>	<333 to W1	(Word mode	)			
	Before Instruction W1 12D0 SR 0000		After Instruction W1 0210 SR 0000						

		AND Wb ar	a Snort Lite	rai		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	AND{.B}	Wb,	#lit5,	Wd	
					[Wd]	
					[Wd++]	
					[Wd]	
					[++Wd]	
					[Wd]	
Operands:	Wb $\in$ [W0					
	lit5 ∈ [0 Wd ∈ [W0	-				
Operation:	(Wb).AND	-				
Status Affected:	N, Z					
Encoding:	0110	0www	wBqq	qddd	d11k	kkkk
Description:	Compute t	he logical AN	D operation o	of the content	s of the base	register
		e 5-bit literal a				
		rect addressi dressing may			Either registe	r direct or
		s select the ac selects byte c		•		vte).
	The 'q' bits	select the de	stination Add	lress mode.	· ·	, ,
		select the de provide the li			togor numbo	r
	Note:	The extension			-	
	NOLE.	rather than a denote a wor	word opera	tion. You may	yusea.We	-
Words:	1		•			
Cycles:	1					
Cycles: <u>Example 1:</u>		,#0x3,[W1++		0 and 0x3 (	Byte mode)	
-		,#0x3,[W1++	; Store	0 and 0x3 ( to [W1] increment W		
-		,#0x3,[W1++	; Store	to [W1]		
-	AND.B W0 Before Instruction		; Store ; Post- After Instructio	to [W1] increment W		
-	AND.B W0 Before Instruction W0 23A5	1	; Store ; Post- After Instructio W0 23A5	to [W1] increment W		
Example 1:	AND.B W0 Before Instruction W0 23A5 W1 2211	1	; Store ; Post- After Instructio W0 23A5 W1 2212	to [W1] increment W		
-	AND.B W0 Before Instruction W0 23A5 W1 2211 2210 9999	1	; Store ; Post- Instructio W0 23A5 W1 2212 210 0199	to [W1] increment W		
Example 1: Data 2	AND . B W0 Before Instruction W0 23A5 W1 2211 2210 9999 SR 0000	Data 2	; Store ; Post- After Instructio W0 23A5 W1 2212 210 0199 SR 0000	to [W1] increment W N	1	
Example 1:	AND.B W0 Before Instruction W0 23A5 W1 2211 2210 9999	1	; Store ; Post- After Instructio W0 23A5 W1 2212 210 0199 SR 0000 ; AND V	to [W1] increment W	1	2)
Example 1: Data 2	AND . B 6000 Before Instruction W0 23A5 W1 2211 2210 9999 SR 0000 AND Before	Data 2 W0, #0×1F, W1	; Store ; Post- After Instructio W0 23A5 W1 2212 210 0199 SR 0000 ; AND V ; Store After	to [W1] increment W N N0 and 0x1F e to W1	1	2)
Example 1: Data 2	AND.B W0 Before Instruction W0 23A5 W1 2211 2210 9999 SR 0000 AND Before Instruction	Data 2 W0, #0x1F, W1	; Store ; Post- After Instructio W0 23A5 W1 2212 210 0199 SR 0000 ; AND V ; Store After Instructior	to [W1] increment W N N0 and 0x1F e to W1	1	2)
Example 1: Data 2	AND . B 6000 Before Instruction W0 23A5 W1 2211 2210 9999 SR 0000 AND Before	Data 2 W0, #0x1F, W1	; Store ; Post- After Instructio W0 23A5 W1 2212 210 0199 SR 0000 ; AND V ; Store After	to [W1] increment W N N0 and 0x1F e to W1	1	3)

AND			And Wb and	d Ws					
Implement	ted in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
		Х	Х	Х	Х	Х	Х		
Syntax:		{label:}	AND{.B}	Wb,	Ws,	Wd			
					[Ws],	[Wd]			
					[Ws++],	[Wd++]			
					[Ws],	[Wd]			
					[++Ws],	[++Wd]			
					[Ws],	[Wd]			
Operands:	:	Wb ∈ [W0 Ws ∈ [W0 Wd ∈ [W0	W15]						
Operation:	:	(Wb).AND.	(Ws) →Wd						
Status Affe	ected:	N, Z							
Encoding:		0110	0www	wBqq	qddd	dppp	SSSS		
Description	n:	Compute the logical AND operation of the contents of the source register Ws and the contents of the base register Wb, and place the result in the destination register Wd. Register direct addressing must be used for Wb. Either register direct or indirect addressing may be used for Ws and Wd.							
		The 'B' bits The 'q' bits The 'd' bits The 'p' bits	select the ad selects byte o select the de select the de select the so select the so	r word operat stination Add stination regis urce Address	tion ('0' for w ress mode. ster.		rte).		
			The extensio rather than a denote a wor	word operation	ion. You may	yuse a.We			
		1							
Words:		1(1)							

# **16-bit MCU and DSC Programmer's Reference Manual**

Example 1:	AND.B	W0,	W1 [W2++]	; AND W0 and W1, and ; store to [W2] (Byte mode) ; Post-increment W2
	Before			After
	Instructio	n		Instruction
	W0 AA55		W	V0 AA55
	W1 2211		W	V1 2211
	W2 1001		W	V2 1002
Data	1000 FFFF		Data 100	
	SR 0000	_	S	SR 0000
Example 2:	AND	W0,	[W1++], W2	2 ; AND WO and [W1], and
				; store to W2 (Word mode)
				; Post-increment W1
	Before			After
	Instructio	n		Instruction
	W0 AA55		W	V0 AA55
	W1 1000		W	V1 1002
	W2 55AA		W	V2 2214
Data	1000 2634		Data 100	00 2634
	SR 0000			SR 0000
	0000	J	0	

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	ASR{.B}	f	{,WREG}		
Operands:	f∈ [0 81	191]				
Operation:	(f<7>) (f<6:1>) (f<0>) <u>For word o</u> (f<15>) - (f<15>)	<pre>&gt;Dest&lt;7&gt; &gt;Dest&lt;6&gt; →Dest&lt;5:0&gt; &gt;C peration: →Dest&lt;15&gt; →Dest&lt;14&gt; </pre>	>			
Status Affected:	N, Z, C					
Encoding:	1101	0101	1BDf	ffff	ffff	ffff
Description:	in the desti shifted into performed, determines stored in W register. The 'B' bit The 'D' bit	ontents of the fi ination register the Carry bit of the result is s the destination VREG. If WREC selects byte or selects the des select the add	The Least s of the STATL ign-extended in register. If G is not spec word opera stination ('0'	Significant bi JS Register. / d. The option WREG is sp cified, the res tion ('0' for w for WREG, '1	t of the file re After the shif al WREG op ecified, the r ult is stored ord, '1' for b	egister is t is erand esult is in the file yte).
	Note 1:	The extension rather than a v denote a word The WREG is	. B in the ins vord operation operation, b	struction den on. You may out it is not re	use a .W ext quired.	
Words:	1					
worus.						

**Note 1:** In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see **Note 3** in **Section 3.2.1 "Multi-Cycle Instructions"**.

ASR.B RAM400, WREG

Example 1:

	; (Byte mode)
Before	After
Instruction	Instruction
WREG 0600	WREG 0611
RAM400 0823	RAM400 0823
SR 0000	SR 0001 (C = 1)
Example 2: ASR RAM200	; ASR RAM200 (Word mode)
Before	After
Instruction	Instruction
RAM200 8009	RAM200 C004
SR 0000	SR 0009 (N, C = 1)

; ASR RAM400 and store to WREG

Implemented in	: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
·	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	ASR{.B}	Ws,	Wd		
Jymax.	(Inc		W3, [Ws],	[Wd]		
			[WS]; [WS++],	[Wd] [Wd++]		
			[Ws],	[Wd]		
			[++Ws],	[++Wd]		
			[Ws],	[Wd]		
Operands:	Ws ∈ [W0 . Wd ∈ [W0 .					
Operation:	(Ws<7>) (Ws<6:1: (Ws<0>) <u>For word op</u> (Ws<15> (Ws<15>	→Wd<7> →Wd<6> >) →Wd<5:0> →C				
	(W3<14 (Ws<0>)		0>			
Status Affected	(Ws<0>)	→C				
Status Affected	(Ws<0>)	→C ►C 0001	1Bqq	qddd	dppp	SSSS
	(Ws<0>) N, Z, C 1101 Shift the course result in the shifted into the result is be used for The 'B' bits The 'q' bits The 'd' bits The 'p' bits	→C _→C	1Bqq source registe egister Wd. T of the STATUS ed. Either regis r word operat stination Addr stination regis urce Address	er Ws one bit to 'he Least Sigr S register. After ster direct or i tion ('0' for wo ress mode. ster.	o the right an hificant bit of er the shift is j indirect addre	d place the Ws is performed, essing may
Encoding:	(Ws<0>) N, Z, C 1101 Shift the conresult in the shifted into the result is be used for The 'B' bits The 'q' bits The 'q' bits The 's' bits The 's' bits	→C 0001 ntents of the s destination re the Carry bit of sign-extende Ws and Wd. selects byte or select the des select the des select the des	1Bqq source registe egister Wd. T of the STATUS ed. Either register tr word operat stination Address urce Address urce register. n . B in the word operat	r Ws one bit to 'he Least Sigr S register. After ster direct or i tion ('0' for wo ress mode. ster. mode. instruction de tion. You may	o the right and hificant bit of er the shift is j indirect addre ord, '1' for byte enotes a byte v use a .W e	d place the Ws is performed, essing may e).
Encoding:	(Ws<0>) N, Z, C 1101 Shift the conresult in the shifted into the result is be used for The 'B' bits The 'q' bits The 'q' bits The 's' bits The 's' bits	→C 0001 ntents of the s destination re the Carry bit of sign-extende Ws and Wd. selects byte or select the des select the des select the sou select the sou select the sou select the sou select the sou select the sou	1Bqq source registe egister Wd. T of the STATUS ed. Either register tr word operat stination Address urce Address urce register. n . B in the word operat	r Ws one bit to 'he Least Sigr S register. After ster direct or i tion ('0' for wo ress mode. ster. mode. instruction de tion. You may	o the right and hificant bit of er the shift is j indirect addre ord, '1' for byte enotes a byte v use a .W e	d place the Ws is performed essing may e).

Example 1:	ASR.B	[W0++],	[W1++]	; ASR [W0] and store to [W1] (Byte mode) ; Post-increment W0 and W1
	Be	efore		After
	Inst	ruction	I	Instruction
	W0	0600	W0	0601
	W1	0801	W1	0802
Data	600	2366	Data 600	2366
Data	. 800 I	FFC0	Data 800	33C0
	SR	0000	SR	0000
Example 2:	ASR N	W12, W13		; ASR W12 and store to W13 (Word mode)
	В	efore		After
	Inst	truction		Instruction
	W13	AB01 0322 0000	W1 W1 SF	3 D580

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
·····	X	X	X	X	X	X
Syntax:	{label:}	ASR	Wb,	#lit4,	Wnd	
Operands:	Wb ∈ [W0 . lit4 ∈ [015 Wnd ∈ [W0	5]				
Operation:	lit4<3:0> $\rightarrow$ Wb<15> $\rightarrow$	-				
Status Affected:	N, Z					
Encoding:	1101	1110	1www	wddd	d100	kkkk
Description:	unsigned lit the shift is p be used for	shift right the o teral, and stor performed, the r Wb and Wno	re the result ir le result is sig d.	n the destinat In-extended.	tion register Direct addres	Wnd. After
	The 'd' bits	s select the ad select the des provide the lit	estination regis	ster.	:	
	Note:	This instruction	on operates ir	n Word mode	e only.	
Words:	1					
Cycles:	1					
Example 1:	ASR W0, #0x4	1, W1	; ASR W0	) by 4 and s	store to W1	
	Before Instruction W0 060F W1 1234 SR 0000	V	After Instruction W0 060F W1 0060 SR 0000			
Example 2:	ASR W0, #0x6	;, W1	; ASR W0	by 6 and s	store to W1	
	Before Instruction W0 80FF W1 0060 SR 0000	W	After Instruction V0 80FF V1 FE03 SR 0008 (I	(N = 1)		
Example 3:	ASR W0, #0×F	7, W1	; ASR W0	) by 15 and	store to h	<i>l</i> 1
	Before Instruction W0 70FF W1 CC26 SR 0000	V	After Instruction W0 70FF W1 0000 SR 0002	(Z = 1)		

ASR		Arithmetic	Shift Right b	y Wns		
Implemented in	: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	ASR	Wb,	Wns,	Wnd	
Operands:	Wb ∈ [W0 Wns ∈ [W0 Wnd ∈ [W0	W15]				
Operation:		→Shift_Val Wnd<15:15-S ft_Val> →Wn				
Status Affected:	: N, Z					
Encoding:	1101	1110	1www	wddd	d000	SSSS
	sign-extend The 'w' bits The 'd' bits The 's' bits Note 1: 2:	register Wnd led. Direct ad select the ac select the de select the so This instruction f Wns is great	dressing mu Idress of the stination regi urce register. on operates in ater than 15,	st be used for base register ster. n Word mode Wnd = 0x0 if	r Wb, Wns ar r. e only.	nd Wnd.
Words:	1	Wnd = 0xFFF	F II WD IS NE	gauve.		
Cycles:	1					
Cycles.	Ŧ					
Example 1:	ASR W0, W5,	W6	; ASR W	0 by W5 and	store to W	16
	Before           Instruction           W0         80FF           W5         0004           W6         2633           SR         0000	N N	After Instruction W0 80FF W5 0004 W6 F80F SR 0000			
Example 2:	ASR W0, W5,	W6	; ASR W	10 by W5 and	d store to N	W6
	Before Instruction W0 6688 W5 000A W6 FF00 SR 0000		After Instructio W0 6688 W5 000A W6 0019 SR 0000			
Example 3:	ASR W11, W1	2, W13	; ASR W	11 by W12 a	ind store to	W13
	Before Instruction W11 8765 W12 88E4 W13 A5A5 SR 0000	Vi Vi	After Instructio /11 8765 /12 88E4 /13 F876 SR 0008			

BCLR		Bit Clear f				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	BCLR{.B}	f,	#bit4		
Operands:	f ∈ [0 81 bit4 ∈ [0	$f \in [0 \dots 8191]$ for byte operation $f \in [0 \dots 8190]$ (even only) for word operation $bit4 \in [0 \dots 7]$ for byte operation $bit4 \in [0 \dots 15]$ for byte operation				
Operation:	0 →f <bit4></bit4>	<b>&gt;</b>				
Status Affected:	None					
Encoding:	1010	1001	bbbf	ffff	ffff	fffb
Description:	Clear the bit in the file register f specified by 'bit4'. Bit numbering begins with the Least Significant bit (bit 0) and advances to the Most Significant bit (bit 7 for byte operations, bit 15 for word operations).					
		select value b select the add			e cleared.	
	2:	<b>Note 1:</b> The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a . W extension to denote a word operation, but it is not required.			ension to	
		When this inst between 0 and	•	ates in Byte n	node, 'bit4' n	nust be
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-mo	dify-write ope	24E devices, t erations on nor Section 3.2.1	n-CPU Specia	al Function R	egisters. For	

Example 1:	BCLR.B 0x800,	#0x7 ; Clear bit 7 in 0x800
Data	Before Instruction 0800 66EF SR 0000	After Instruction Data 0800 666F SR 0000
Example 2:	BCLR 0x400,	#0x9 ; Clear bit 9 in 0x400
Data	Before Instruction 0400 AA55 SR 0000	After Instruction Data 0400 A855 SR 0000

BCLR		Bit Clear in	Ws				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	BCLR{.B}	Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws],	#bit4			
Operands:		W15] 7] for byte op 15] for word o					
Operation:	0 →Ws <bit< td=""><td>4&gt;</td><td></td><td></td><td></td><td></td></bit<>	4>					
Status Affected:	None						
Encoding:	1010	0001	bbbb	0B00	0ppp	SSSS	
Description:	Clear the bit in register Ws specified by 'bit4'. Bit numbering begins with the Least Significant bit (bit 0) and advances to the Most Significant bit (bi 7 for byte operations, bit 15 for word operations). Register direct or indirect addressing may be used for Ws. The 'b' bits select value bit4 of the bit position to be cleared. The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 's' bits select the source/destination register. The 'p' bits select the source Address mode.					cant bit (bit	
						yte).	
	<b>Note 1:</b> The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a . W extension denote a word operation, but it is not required.				ension to		
		When this inst egister addre	-			burce	
	<ul><li>3: When this instruction operates in Byte mode, 'bit4' must be between 0 and 7.</li></ul>						
	4: I	n dsPIC33E a DSRPAG regi Data Space.	and PIC24E	·			
Words:	1						
Cycles:	1 <sup>(1)</sup>						

**Note 1:** In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see **Note 3** in **Section 3.2.1** "Multi-Cycle Instructions".

Example 1:	BCLR.B W2, #0x2	; Clear bit 3 in W2
	Before Instruction W2 F234 SR 0000	After Instruction W2 F230 SR 0000
Example 2:	BCLR [W0++], #0×0	; Clear bit 0 in [W0] ; Post-increment W0
	Before Instruction W0 2300	After Instruction W0 2302
Data		w0         2302           ata 2300         5606           SR         0000

BRA	I	Branch Unco	onditionally			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	BRA	Expr			
Operands:	Expr may be Expr is resolv					+32767].
Operation:	(PC + 2) + 2 N0P →Instruc					
Status Affected:	None					
Encoding:	0011	0111	nnnn	nnnn	nnnn	nnnn
Description:	The program of the branch branches up resolved by t expression. A Slit16, since The 'n' bits a offset from (F	i is the two's to 32K instru he linker fron After the bran the PC will ha re a signed li	complement i ctions forward n the supplied ch is taken, th ave incremen	number '2 * S d or backward I label, absolu ne new addre ted to fetch th	slit16', which d. The Slit16 ute address o ss will be (P0 ne next instru	supports value is or C + 2) + 2 * iction.
Words:	1					
Cycles:	2 (PIC24F, P 4 (PIC24E, d		C30F, dsPIC3	3F)		
Example 1:	002000 HERE: 002002 002004 002006 002008 002008 THERE 00200C	BRA THE     	RE	; В	ranch to TH	IERE
	Before Instructio PC 00 20 SR 00	on 00	PC SR	After Instruction 00 200A 0000		
Example 2:	002000 HERE: 002002 002004 002006 002008 00200A THERE: 00200C	BRA THER     	RE+0x2	; Br	anch to THE	RE+0x2
	Before Instruction PC 00 200 SR 000	0	PC SR	After Instruction 00 200C 0000		

Example 3:	002000 HERE: 002002 002004	BRA 0×1366  	
	Before		Aft

Instruction

00 2000

0000

PC

SR

; Branch to 0x1366

	After
	Instruction
PC	00 1366
SR	0000

BRA		Computed E	Branch			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х		Х	Х	
Syntax:	{label:}	BRA	Wn			
Operands:	Wn∈ [W	0 W15]				
Operation:		+ (2 * Wn) →PC struction Registe				
Status Affected:	None					
Encoding:	0000	0001	0110	0000	0000	SSSS
	executes incremen	up to 32K instru , the new PC wi ted to fetch the ts select the sou	II be (PC + 2) next instruction	+ 2 * Wn, si		
Words:	1					
Cycles:	2					
<u>Example 1:</u>	002000 HERE: 002002  002108 00210A TABLE 00210C	· · · · · · · · · ·	;	Branch for	ward (2+2*	W7)
		on	 PC   W7   SR	After nstruction 00 210A 0084 0000		

BRA		Computed I	Branch					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
			Х			Х		
Syntax:	{label:}	BRA	Wn					
Operands:	Wn∈ [W0	W15]						
Operation:		(PC + 2) + (2 * Wn) →PC NOP →Instruction Register						
Status Affected:	None							
Encoding:	0000	0001	0000	0110	0000	SSSS		
Description:	of the bran branches of executes, incremente The 's' bits	The program branches unconditionally, relative to the next PC. The offset of the branch is the sign-extended 17-bit value (2 * Wn), which supports branches up to 32K instructions forward or backward. After this instruction executes, the new PC will be (PC + 2) + 2 * Wn, since the PC will have incremented to fetch the next instruction. The 's' bits select the source register.						
Words:	1							
Cycles:	4							
Example 1:	002000 HERE: 002002  002108 00210A TABLE 00210C	BRA W7	;	Branch for	ward (2+2*	W7)		
	Before Instructio PC 00 200 W7 000 SR 000	00 84	PC W7 SR	After nstruction 00 210A 0084 0000				

BRA C		Branch if Ca	ırry					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	BRA	С,	Expr				
Operands:		Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].						
Operation:	If (Condition (PC + 2)	Condition = C If (Condition) (PC + 2) + 2 * Slit16 →PC NOP →Instruction Register						
Status Affected:	None							
Encoding:	0011	0001	nnnn	nnnn	nnnn	nnnn		
	The offset of the branch is the two's complement number '2 * Slit16', which supports branches up to 32K instructions forward or backward. The Slit16 value is resolved by the linker from the supplied label, absolute address or expression. If the branch is taken, the new address will be (PC + 2) + 2 * Slit16, since the PC will have incremented to fetch the next instruction. The instruction then							
		two-cycle instr are a 16-bit siç vords				-		
Words:	1							
Cycles:	1 (2 if branc	h taken) – PIC	24F, PIC24H,	dsPIC30F, d	IsPIC33F			
	1 (4 if branc	h taken) – PIC	24E, dsPIC33	BE				
	002000 HERE: 002002 NO_C: 002004 002006 002008 CARRY: 00200A 00200C THERE: 00200E		;	If C is set Otherwise				
	Before Instruction PC 00 200 SR 000		PC SR	After nstruction 00 2008 0001 (0	C = 1)			



BRA GE		Branch if Signed Greater Than or Equal						
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	BRA	GE,	Expr				
Operands:	Expr is reso	Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].						
Operation:	If (Condition (PC + 2)	Condition = $(N\&OV)  (!N\&@OV)$ If (Condition) $(PC + 2) + 2 * Slit16 \rightarrow PC$ NOP $\rightarrow$ Instruction Register						
Status Affected:	None							
Encoding:	0011	1101	nnnn	nnnn	nnnn	nnnn		
	Description:If the logical expression (N&&OV)  (!N&&!OV) is true, then the progra will branch relative to the next PC. The offset of the branch is the two complement number '2 * Slit16', which supports branches up to 32K instructions forward or backward. The Slit16 value is resolved by the linker from the supplied label, absolute address or expression.If the branch is taken, the new address will be (PC + 2) + 2 * Slit16, s							
	the PC will then becom cycle.	have increme nes a two-cyc	ented to fetch le instruction	n the next inst n, with a NOP	truction. The executed in t	instruction he second		
	The 'n' bits in instructio	are a 16-bit s n words.	signed literal	that specify t	he offset fror	n (PC + 2)		
		The assembl be used.	er will conve	r will convert the specified label into the offset to				
Words:	1							
Cycles:	1 (2 if brand	ch taken) – P	IC24F, PIC24	4H, dsPIC30F	, dsPIC33F			
	1 (4 if brand	ch taken) – P	IC24E, dsPI	C33E				
0 0 0 0 0	07600 LOOP: 07602 07604 07606 07608 HERE: 0760A NO_GE:	   BRA GE, Lu	00P		branch to .se cont			
	Before Instruction PC 00 7608 SR 0000	]	PC SR	After nstruction 00 7600 0000				

Example 2:	007600 LOOP: 007602 007604 007606	· · · · · ·	
	007608 HERE: 00760A NO_GE:	BRA GE, LOOP	; If GE, branch to LOO ; Otherwise continu
	Before		After
	Instruction		Instruction
	PC 00 7608		PC 00 760A
	SR 0008	(N = 1)	SR 0008 (N = 1)

\_ \_ . .

BRA G	Branch if Unsigned Greater Than or Equal							
Implemented in	1:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
		Х	Х	Х	Х	Х	Х	
Syntax:		{label:}	BRA	GEU,	Expr			
Operands:		Expr is res	be a label, at solved by the 32768 +32	linker to a S	lit16 offset th		an offset	
Operation:		If (Condition (PC + 2)	Condition = C If (Condition) (PC + 2) + 2 * Slit16 →PC NOP →Instruction Register					
Status Affected	:	None						
Encoding:		0011	0001	nnnn	nnnn	nnnn	nnnn	
Description:		If the Carry flag is '1', then the program will branch relative to the next PC. The offset of the branch is the two's complement number '2 * Slit16', which supports branches up to 32K instructions forward or backward. The Slit16 value is resolved by the linker from the supplied label, absolute address or expression.						
		If the branch is taken, the new address will be $(PC + 2) + 2 * Slit16$ , since the PC will have incremented to fetch the next instruction. The instruction then becomes a two-cycle instruction, with a NOP executed in the second cycle.						
		The 'n' bits are a 16-bit signed literal that specify the offset from (PC + 2) in instruction words.						
		Note:		uction and ha	tical to the I as the same t16.			
Words:		1						
Cycles:		1 (2 if brar	nch taken) – F	PIC24F, PIC	24H, dsPIC3	0F, dsPIC33	F	
		1 (4 if brar	nch taken) – F	PIC24E, dsP	PIC33E			
Example 1:	002004 002006 002008 00200A	NO_GEU: BYPASS:	BRA GEU,   GOTO THER 		; to	C is set, BYPASS erwise		
		Before Instruction 00 2000 0001	(C = 1)	PC SR	After Instruction 00 200C 0001 (C	C = 1)		

BRA G	т	Branch if Signed Greater Than							
Implemented in	n: PIC24	F PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	BRA	GT,	Expr					
Operands:	Expr is	Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].							
Operation:	lf (Conc PC -	Condition = $(!Z\&\&N\&\&OV)  (!Z\&\&!N\&\&!OV)$ If (Condition) (PC + 2) + 2 * Slit16 $\rightarrow$ PC NOP $\rightarrow$ Instruction Register							
Status Affected	l: None								
Encoding:	0011	1100	nnnn	nnnn	nnnn	nnnn			
	two's co instructi linker fr If the br the PC	<ul> <li>program will branch relative to the next PC. The offset of the branch is two's complement number '2 * Slit16', which supports branches up to 3 instructions forward or backward. The Slit16 value is resolved by the linker from the supplied label, absolute address or expression.</li> <li>If the branch is taken, the new address will be (PC + 2) + 2 * Slit16, sir the PC will have incremented to fetch the next instruction. The instruct then becomes a two-cycle instruction, with a NOP executed in the second.</li> </ul>							
	The 'n'	bits are a 16-bit iction words.	signed literal	that specify t	he offset fror	n (PC + 2)			
Words:	1								
Cycles:	1 (2 if b	ranch taken) – I	PIC24F, PIC2	4H, dsPIC30	F, dsPIC33F				
	1 (4 if b	ranch taken) – I	PIC24E, dsPI	C33E					
<u>Example 1:</u>	002000 HERE 002002 NO_0 002004 002006 002008 00200A 00200A 00200C BYPA	GT:  GOTO TH	. BYPASS HERE	,	GT, branch erwise c				
			PC SR	After Instruction 00 200C 0001 (C	:= 1)				

BRA GIU	J	Branch if U	nsigned Gre	ater Than			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	BRA	GTU,	Expr			
Operands:	Expr is reso	Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].					
Operation:	If (Condition (PC + 2)	Condition = (C&&!Z) If (Condition) (PC + 2) + 2 * Slit16 $\rightarrow$ PC NOP $\rightarrow$ Instruction Register					
Status Affected:	None						
Encoding:	0011	1110	nnnn	nnnn	nnnn	nnnn	
forward or backward. The Slit16 value is resolved by the lin supplied label, absolute address or expression. If the branch is taken, the new address will be (PC + 2) + 2 the PC will have incremented to fetch the next instruction. T then becomes a two-cycle instruction, with a NOP executed					C + 2) + 2 * S truction. The	lit16, since instruction	
	cycle. The 'n' bits offset from	are a signed (PC + 2).	literal that sp	pecifies the n	umber of inst	tructions	
Words:	1						
Cycles:	1 (2 if bran	ch taken) – P	IC24F, PIC24	4H, dsPIC30F	F, dsPIC33F		
	1 (4 if bran	ch taken) – P	IC24E, dsPI	C33E			
002 002 002 002 002 002 002	2000 HERE: 2002 NO_GTU: 2004 2006 2008 200A 200C BYPASS: 200E	BRA GTU,   GOTO THEN		,	J, branch t vise con		
PC		(C = 1)	Inst	After ruction 00 200C 0001 (C =	: 1)		

#### BRAGTU Branch if Unsigned Greater Than

BRA L	Е	Branch if Signed Less Than or Equal							
Implemented	in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
		Х	Х	Х	Х	Х	Х		
Syntax:		{label:}	BRA	LE,	Expr				
Operands:		Expr is reso	Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].						
Operation:		If (Condition (PC + 2)	Condition = Z  (N&&!OV)  (!N&&OV) f (Condition) (PC + 2) + 2 * Slit16 →PC N0P →Instruction Register						
Status Affecte	ed:	None							
Encoding:		0011	0100	nnnn	nnnn	nnnn	nnnn		
	<ul> <li>program will branch relative to the next PC. The offset of the branch two's complement number '2 * Slit16', which supports branches up to instructions forward or backward. The Slit16 value is resolved by the from the supplied label, absolute address or expression.</li> <li>If the branch is taken, the new address will be (PC + 2) + 2 * Slit16, the PC will have incremented to fetch the next instruction. The instruction becomes a two-cycle instruction, with a NOP executed in the se cycle.</li> </ul>						to 32K y the linker it16, since instruction		
		The 'n' bits offset from	are a signed (PC + 2).	literal that sp	pecifies the n	umber of inst	ructions		
Words:		1							
Cycles:		1 (2 if brand	ch taken) – P	IC24F, PIC24	4H, dsPIC30F	F, dsPIC33F			
		1 (4 if brand	ch taken) – P	IC24E, dsPI0	C33E				
Example 1:	0020 0020 0020 0020 0020	006 008 00A 00C BYPASS:	BRA LE,   GOTO THE 			LE, branch nerwise			
	PC SR	Before Instruction 00 2000	) (C = 1)	PC SR	After Instruction 00 2002 0001 (	C = 1)			

	EU	Branch if U	nsigned Les	s Than or E	quai			
Implemented i	n: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	BRA	LEU,	Expr				
Operands:	Expr is res	Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].						
Operation:	If (Conditio (PC + 2)	Condition = $ C  Z$ If (Condition) (PC + 2) + 2 * Slit16 $\rightarrow$ PC NOP $\rightarrow$ Instruction Register						
Status Affecte	d: None							
Encoding:	0011	0110	nnnn	nnnn	nnnn	nnnn		
forward or backward. The Slit16 value is resolved by the linker supplied label, absolute address or expression. If the branch is taken, the new address will be (PC + 2) + 2 * S the PC will have incremented to fetch the next instruction. The then becomes a two-cycle instruction, with a NOP executed in t					lit16, since instruction			
	cycle. The 'n' bits offset from	are a signed (PC + 2).	literal that sp	pecifies the n	umber of inst	ructions		
Words:	1							
Cycles:	1 (2 if bran	ich taken) – P	IC24F, PIC24	4H, dsPIC30I	=, dsPIC33F			
	1 (4 if bran	ich taken) – P	IC24E, dsPI	C33E				
Example 1:	002000 HERE: 002002 NO_LEU 002004 002006 002008 00200A 00200C BYPASS 00200E	  GOTO ТНЕ			EU, branch rwise cc			
	Before Instruction PC 00 200 SR 000		PC SR	After struction 00 200C 0001 (C	= 1)			

#### BRALEU Branch if Unsigned Less Than or Equal

BRA L	Г	Branch if S	igned Less	Than			
Implemented in	n: PIC24	F PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	BRA	LT,	Expr			
Operands:	Expr is r	Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].					
Operation:	lf (Cond (PC +	Condition = $(N\&\&!OV)  (!N\&\&OV)$ If (Condition) $(PC + 2) + 2 * Slit16 \rightarrow PC$ NOP $\rightarrow$ Instruction Register					
Status Affected	d: None						
Encoding:	0011	0101	nnnn	nnnn	nnnn	nnnn	
	<ul> <li>will branch relative to the next PC. The offset of the branch is the two complement number '2 * Slit16', which supports branches up to 32K instructions forward or backward. The Slit16 value is resolved by the linker from the supplied label, absolute address or expression.</li> <li>If the branch is taken, the new address will be (PC + 2) + 2 * Slit16, s the PC will have incremented to fetch the next instruction. The instruction becomes a two-cycle instruction, with a NOP executed in the sec cycle.</li> </ul>					o 32K by the lit16, since instruction	
		oits are a signed om (PC + 2).	literal that s	pecifies the n	umber of inst	ructions	
Words:	1						
Cycles:	1 (2 if br	anch taken) – P	PIC24F, PIC2	4H, dsPIC30I	F, dsPIC33F		
	1 (4 if br	anch taken) – F	PIC24E, dsPI	C33E			
<u>Example 1:</u>	002000 HERE 002002 NO_L 002004 002006 002008 00200A 00200C BYPA 00200E	Т:   GOTO ТН	BYPASS ERE	,	T, branch t rwise cc		
	Before Instruct PC 00 2 SR 0	ion	PC SR	After struction 00 2002 0001 (C	= 1)		

BRA LTI	J	Branch if Unsigned Less Than							
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	BRA	LTU,	Expr					
Operands:	Expr is res	Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].							
Operation:	If (Conditio (PC + 2)	Condition = $!C$ If (Condition) (PC + 2) + 2 * Slit16 $\rightarrow$ PC NOP $\rightarrow$ Instruction Register							
Status Affected:	None								
Encoding:	0011	1001	nnnn	nnnn	nnnn	nnnn			
Description:	The offset of which supp Slit16 value	If the Carry flag is '0', then the program will branch relative to the next PC. The offset of the branch is the two's complement number '2 * Slit16', which supports branches up to 32K instructions forward or backward. The Slit16 value is resolved by the linker from the supplied label, absolute address or expression.							
	the PC will	If the branch is taken, the new address will be (PC + 2) + 2 * Slit16, since the PC will have incremented to fetch the next instruction. The instruction then becomes a two-cycle instruction, with a NOP executed in the second cycle.							
	The 'n' bits offset from	are a signed (PC + 2).	literal that sp	pecifies the n	umber of ins	tructions			
		This instructio Carry) instruc assemble as	tion and has	the same en	• •				
Words:	1								
Cycles:	1 (2 if bran	ch taken) – P	IC24F, PIC24	4H, dsPIC30I	F, dsPIC33F				
	1 (4 if bran	ch taken) – P	IC24E, dsPI	C33E					
00 00 00 00 00 00 00 00	22000 HERE: 22002 NO_LTU: 22004 22006 22008 22008 22000 BYPASS: 2200E	BRA LTU,   GOTO THE 			Ū, branch ™ise co				
P S		(C = 1)		After struction 00 2002 0001 (C	= 1)				

BRA N		E	Branch if Ne	egative					
Implemented	in: PIC2	4F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х		Х	Х	Х	Х	Х		
Syntax:	{label:}	ьE	BRA	N,	Expr				
Operands:	Expr is	Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].							
Operation:	lf (Con (PC	Condition = N If (Condition) (PC + 2) + 2 * Slit16 $\rightarrow$ PC NOP $\rightarrow$ Instruction Register.							
Status Affecte	d: None								
Encoding:	001	1	0011	nnnn	nnnn	nnnn	nnnn		
Slit16 value is resolved by the link address or expression. If the branch is taken, the new add the PC will have incremented to fe					32K instructions forward or backward. The linker from the supplied label, absolute address will be (PC + 2) + 2 * Slit16, since o fetch the next instruction. The instruction ruction, with a NOP executed in the second				
			re a signed PC + 2).	literal that sp	ecifies the n	umber of inst	ructions		
Words:	1								
Cycles:	1 (2 if l	1 (2 if branch taken) – PIC24F, PIC24H, dsPIC30F, dsPIC33F							
1 (4 if branch taken) – PIC24E, dsPIC33E									
<u>Example 1:</u>	002000 HER 002002 NO_ 002004 002006 002008 00200A 00200C BYP 00200E	N:	BRA N, E   GOTO THE 			N, branch t erwise c			
		ction 2000	(N = 1)	Ir PC SR	After Istruction 00 200C 0008 (N	= 1)			

BRA N	C	Branch if N	lot Carry					
Implemented	in: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	BRA	NC,	Expr				
Operands:	Expr is re	Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].						
Operation:	If (Condit (PC +	Condition = !C If (Condition) (PC + 2) + 2 * Slit16 →PC NOP →Instruction Register						
Status Affecte	d: None							
Encoding:	0011	1001	nnnn	nnnn	nnnn	nnnn		
	expression If the bra the PC w then beco	value is resolved by the linker from the supplied label, absolute address or expression. If the branch is taken, the new address will be $(PC + 2) + 2 * Slit16$ , since the PC will have incremented to fetch the next instruction. The instruction then becomes a two-cycle instruction, with a NOP executed in the second						
	The 'n' bi	cycle. The 'n' bits are a signed literal that specifies the number of instructions offset from (PC + 2).						
Words: 1								
Cycles:	– 1 (2 if branch taken) – PIC24F, PIC24H, dsPIC30F, dsPIC33F							
1 (4 if branch taken) – PIC24E, dsPIC33E								
<u>Example 1:</u>	002000 HERE: 002002 NO_NC 002004 002006 002008 00200A 00200C BYPAS: 00200E	  GOTO THI			;, branch to wise co			
	Before Instructio PC 00 20 SR 00			After struction 00 2002 0001 (C :	= 1)			

Implemented	in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
		Х	Х	Х	Х	Х	Х		
Syntax:		{label:}	BRA	NN,	Expr				
Operands:		Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].							
Operation:		Condition = !N If (Condition) (PC + 2) + 2 * Slit16 →PC NOP →Instruction Register							
Status Affecte	ed:	None							
Encoding:		0011	1011	nnnn	nnnn	nnnn	nnnn		
		<ul><li>Slit16 value is resolved by the linker from the supplied label, absolute address or expression.</li><li>If the branch is taken, the new address will be (PC + 2) + 2 * Slit16, since the PC will have incremented to fetch the next instruction. The instruction then becomes a two-cycle instruction, with a NOP executed in the second</li></ul>							
		cycle. The 'n' bits are a signed literal that specifies the number of instructions offset from (PC + 2).							
Words:		1	( - )						
Cycles:		1 (2 if brand	ch taken) – P	IC24F, PIC24	4H, dsPIC30F	F, dsPIC33F			
		1 (4 if brand	ch taken) – P	IC24E, dsPlo	C33E				
Example 1:	00200 00200 00200 00200 00200	06 08 0A 0C BYPASS:	BRA NN,   GOTO THE 			branch to ise cont			
	PC SR	Before Instruction 00 2000 0000		Inst	fter ruction 0 200C 0000				

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BRA N	ÖV	Branch if N	ot Overflow						
Implemented i	n: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	BRA	NOV,	Expr					
Operands:	Expr is re	Expr may be a label, absolute address or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].							
Operation:	If (Conditi (PC + 2	Condition = $!OV$ If (Condition) (PC + 2) + 2 * Slit16 $\rightarrow$ PC NOP $\rightarrow$ Instruction Register							
Status Affecte	d: None								
Encoding:	0011	1000	nnnn	nnnn	nnnn	nnnn			
	address o If the brar the PC wi then beco	Slit16 value is resolved by the linker from the supplied label, absolute address or expression. If the branch is taken, the new address will be $(PC + 2) + 2 * Slit16$ , since the PC will have incremented to fetch the next instruction. The instruction then becomes a two-cycle instruction, with a NOP executed in the second							
		cycle. The 'n' bits are a signed literal that specifies the number of instructions offset from (PC + 2).							
Words:	1	<b>、</b>							
Cycles:									
	1 (4 if bra	nch taken) – P	IC24E, dsPIC	C33E					
<u>Example 1:</u>	002000 HERE: 002002 NO_NOV 002004 002006 002008 00200A 00200C BYPASS 00200E	  GOTO THE			V, branch t wise con				
	Before Instruction PC 00 200 SR 000		Ins	After truction 00 200C 0008 (N =	= 1)				

## BRA NOV Branch if Not Overflow
BRA N	IZ		Branch if N	ot Zero			
Implemented	in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	ĺ	Х	Х	Х	Х	Х	Х
Syntax:		{label:}	BRA	NZ,	Expr		
Operands:		Expr is res	be a label, ab olved by the l 2768 +327	inker to a Slit		ion.	
Operation:							
Status Affecte	ed:	None					
Encoding:		0011	1010	nnnn	nnnn	nnnn	nnnn
		supports branches up to 32K instructions forward or backward. The Slit16 value is resolved by the linker from the supplied label, absolute address or expression. If the branch is taken, the new address will be $(PC + 2) + 2 * Slit16$ , since the PC will have incremented to fetch the next instruction. The instruction then becomes a two-cycle instruction, with a NOP executed in the second cycle.					
		The 'n' bits offset from	are a signed (PC + 2).	literal that sp	pecifies the n	umber of inst	ructions
Words:		1					
Cycles:		1 (2 if bran	ch taken) – P	IC24F, PIC24	4H, dsPIC30F	-, dsPIC33F	
		1 (4 if bran	ch taken) – P	IC24E, dsPI	C33E		
Example 1:	00200 00200 00200 00200 00200	96 98 9A 9C BYPASS:	BRA NZ,   GOTO THE 			branch to	
	PC SR	Before Instruction 00 2000 0002	(Z = 1)	Inst	After ruction 00 2002 0002 (Z =	1)	

BRA O	Α		Branch if O	verflow Acc	umulator A		
Implemented i	n:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
					Х	Х	Х
Syntax:		{label:}	BRA	OA,	Expr		
Operands:		Expr is res	be a label, ab olved by the l 32768 +327	inker to a Sli		ion.	
Operation:			-				
Status Affected	d:	None					
Encoding:		0000	1100	nnnn	nnnn	nnnn	nnnn
	<ul> <li>If the Overflow Accumulator A flag is '1', then the program will branch relative to the next PC. The offset of the branch is the two's complement number '2 * Slit16', which supports branches up to 32K instructions forward or backward. The Slit16 value is resolved by the linker from the supplied label, absolute address or expression.</li> <li>If the branch is taken, the new address will be (PC + 2) + 2 * Slit16, since</li> </ul>						tions
		the PC will	ch is taken, th have increments nes a two-cyc	ented to fetch	the next ins	truction. The	instruction
		The 'n' bits offset from	s are a signed (PC + 2).	literal that s	pecifies the n	umber of ins	tructions
		Note:	The assemb be used.	ler will conve	rt the specifie	ed label into t	he offset to
Words:		1					
Cycles:		1 (2 if brar	ich taken) – d	sPIC30F, dsł	PIC33F		
		1 (4 if brar	ıch taken) – d	sPIC33E			
Example 1:	00200 00200 00200 00200 00200	6 8 A C BYPASS:	   GOTO THE	BYPASS RE		, branch to wise co	
	PC SR	Before Instruction 00 2000 8800	) ) (OA, OAB =	Ins PC	After truction 00 200C 8800 (OA	A, OAB = 1)	

BRA C	)B		Branch if O	verflow	Acc	umulator B		
Implemented	in:	PIC24F	PIC24H	PIC24	E	dsPIC30F	dsPIC33F	dsPIC33E
						Х	Х	Х
Syntax:		{label:}	BRA	OB,		Expr		
Operands:		Expr is res	be a label, ab olved by the l 32768 +327	inker to a		•	ion.	
Operation:			-					
Status Affecte	ed:	None						
Encoding:		0000	1101	nnnr	I	nnnn	nnnn	nnnn
		supplied la If the branc the PC will then becon	backward. Th bel, absolute ch is taken, th have increme nes a two-cyc	address e new ad ented to f	or e Idres etch	xpression. ss will be (PC ) the next ins	C + 2) + 2 * S truction. The	lit16, since instruction
		cycle. The 'n' bits offset from	are a signed (PC + 2).	literal tha	at sp	pecifies the n	umber of ins	tructions
Words:		1	<b>`</b>					
Cycles:		1 (2 if bran	ch taken) – d	sPIC30F,	dsF	PIC33F		
		1 (4 if bran	ch taken) – d	sPIC33E				
Example 1:	00200 00200 00200 00200 00200	96 98 9A 9C BYPASS:	BRA OB,   GOTO THE 				8, branch t wise co	
	PC SR	Before Instruction 00 2000 8800	) (OA, OAB =	PC 1) SR	Ins	After truction 00 2002 8800 (OA	A, OAB = 1)	

. .

BRA O	V	Branch if O	verflow				
Implemented i	n: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	BRA	OV,	Expr			
Operands:	Expr is res	be a label, abs solved by the l 32768 +327	inker to a Slit		on.		
Operation:	If (Condition (PC + 2	Condition = OV f (Condition) (PC + 2) + 2 * Slit16 →PC NOP →Instruction Register					
Status Affecte	d: None						
Encoding:	0011	0000	nnnn	nnnn	nnnn	nnnn	
	Slit16 valu address o If the bran the PC wil then beco	ports branches le is resolved l r expression. Ich is taken, th Il have increme mes a two-cyc	by the linker the linker the new address address and the fetch	from the supp ss will be (PC 1 the next inst	lied label, at (+ 2) + 2 * Si ruction. The	osolute lit16, since instruction	
		s are a signed ı (PC + 2).	literal that sp	pecifies the nu	umber of inst	ructions	
Words:	1						
Cycles:	-	nch taken) – P			, dsPIC33F		
	1 (4 if brai	nch taken) – P	IC24E, dsPI0	C33E			
Example 1:	002000 HERE: 002002 NO_OV 002004 002006 002008 002008 00200A 00200C BYPASS 00200E	BRA OV,   GOTO THI S:			, branch to wise col		
	Before Instruction PC 00 200 SR 000			After struction 00 2002 0002 (Z =	= 1)		

BRA S	<b>SA</b>		Branch if S	aturation Ac	cumulator A	۱.	
Implemented	in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
					Х	Х	Х
Syntax:	{la	abel:}	BRA	SA,	Expr		
Operands:	E	xpr is reso	e a label, ab olved by the l 2768 +327	inker to a Sli	ss or express t16, where	ion.	
Operation:	_		-				
Status Affecte	ed: N	one					
Encoding:		0000	1110	nnnn	nnnn	nnnn	nnnn
	fo sı If th	orward or l upplied lal the branc ne PC will	backward. Th bel, absolute h is taken, th have increme	e Slit16 valu address or e e new addre ented to fetcl	ranches up to le is resolved expression. ss will be (PC n the next ins n, with a NOP	by the linker C + 2) + 2 * S truction. The	from the lit16, since instruction
		he 'n' bits ffset from	-	literal that s	pecifies the n	umber of inst	ructions
Words:	1						
Cycles:	1	(2 if brand	ch taken) – d	sPIC30F, dsl	PIC33F		
	1	(4 if brand	ch taken) – d	sPIC33E			
<u>Example 1:</u>	002000 002002 002004 002006 002008 00200A 00200C 00200E		BRA SA,   GOTO THE 			A, branch t wise co	
		Before struction 00 2000 2400	(SA, SAB =	PC	After struction 00 200C 2400 (SA	A, SAB = 1)	

BRA S	В		Branch if S	aturation Ac	cumulator E	3	
Implemented	in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
					Х	Х	Х
Syntax:		{label:}	BRA	SB,	Expr		
Operands:		Expr is res	be a label, ab olved by the l 2768 +327	inker to a Sli		ion.	
Operation:			-				
Status Affecte	ed:	None					
Encoding:		0000	1111	nnnn	nnnn	nnnn	nnnn
		forward or supplied la If the brand the PC will then becom cycle.	* Slit16', whic backward. Th bel, absolute ch is taken, th have increme nes a two-cyc	e Slit16 valu address or e e new addre ented to fetch cle instruction	e is resolved xpression. ss will be (PC the next ins the next ins the NOP	by the linker C + 2) + 2 * S truction. The executed in t	from the lit16, since instruction he second
		The 'n' bits offset from	are a signed (PC + 2).	literal that s	becifies the n	umber of inst	ructions
Words:		1					
Cycles:		1 (2 if bran	ch taken) – d	sPIC30F, dsI	PIC33F		
		1 (4 if bran	ch taken) – d	sPIC33E			
Example 1:	0020 0020 0020 0020 0020	06 08 0A 0C BYPASS:	BRA SB,   GOTO THE 			branch to ise con†	
	PC SR	Before Instruction 00 2000 0000		Inst	fter ruction 00 2002 0000		

BRA Z		Branch if Ze	ero					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	BRA	Ζ,	Expr				
Operands:	Expr is reso	e a label, abs blved by the li 2768 +327	nker to a Slit		on.			
Operation:	(PC + 2)	f (Condition) (PC + 2) + 2 * Slit16 →PC NOP →Instruction Register						
Status Affected:	None							
Encoding:	0011	0010	nnnn	nnnn	nnnn	nnnn		
	the PC will	h is taken, the have increme nes a two-cyc	ented to fetch	the next inst	ruction. The i	nstruction		
	5	are a signed (PC + 2).	literal that sp	ecifies the nu	umber of instr	uctions		
Words:	1	().						
Cycles:	-	ch taken) – Pl			, dsPIC33F			
	1 (4 if brand	ch taken) – Pl	IC24E, dsPIC	:33E				
<u> </u>	002000 HERE: 002002 NO_Z: 002004 002006 002008 002008 002000 BYPASS 00200E	BRA Z,   GOTO TH :			Z, branch t lerwise (			
	Before Instruction PC 00 200 SR 000		PC SR	After nstruction 00 200C 0002 (2	Z = 1)			

BSET	_	Bit Set f				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	BSET{.B}	f,	#bit4		
Operands:	f ∈ [0 81 bit4 ∈ [0	.91] for byte c .90] (even on . 7] for byte o . 15] for word	ly) for word c peration	peration		
Operation:	1 →f <bit4></bit4>					
Status Affected:	None					
Encoding:	1010	1000	bbbf	ffff	ffff	fffb
Description:	with the Le	in the file reg ast Significar r byte operati	nt bit (bit 0) a	nd advances	to the Most	
	The 'b' bits select value bit4 of the bit position to be set. The 'f' bits select the address of the file register.					
	2: 3:	The extensio rather than a denote a wor When this ins address mus When this ins between 0 ar	word operat d operation, struction ope t be word-alig struction ope	ion. You may but it is not re rates in Worc gned.	use a .Wex equired. I mode, the f	tension to ile register
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-mod details, se	lify-write ope	24E devices, rations on no <b>Section 3.2.</b> ., #0x3	n-CPU Speci L "Multi-Cyc	al Function R	egisters. For ns".	
Data 0600 SR		Data 06	After Instruction 00 FA34 5R 0000			
Example 2: BSE	T 0x444	, #0xF	; Set bi	t 15 in 0x4	444	
Data 0444 SR		Data 04	After Instruction 44 D604 6R 0000			

BSET		Bit Set in Ws							
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33			
	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	BSET{.B}	Ws,	#bit4					
			[Ws],						
			[Ws++],						
			[Ws],						
			[++Ws],						
			[Ws],						
Operands:	bit4 ∈ [0	Vs ∈ [W0 W15] it4 ∈ [0 7] for byte operation it4 ∈ [0 15] for word operation							
Operation:	1 →Ws <bit< td=""><td>4&gt;</td><td></td><td></td><td></td><td></td></bit<>	4>							
Status Affected:	None								
Encoding:	1010	0000	bbbb	0B00	0ppp	SSSS			
Description:	Least Sign for byte op	in register Ws ificant bit (bit ( erations, bit 1 may be used	0) and advan 5 for word op	ces to the Mo	ost Significan	t bit (bit 7			
	The 'B' bit The 'p' bits	The 'b' bits select value bit4 of the bit position to be cleared. The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'p' bits select the source Address mode. The 's' bits select the source/destination register.							
		<b>Note 1:</b> The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a . W extension to							
		denote a word operation, but it is not required. When this instruction operates in Word mode, the source register address must be word-aligned.							
	2:	When this ins	truction operation	ates in Word	mode, the so				
	2: 3:	When this ins	truction oper ess must be v truction oper	ates in Word vord-aligned.	mode, the so	ource			
	2: 3: 4:	When this ins register addre When this ins	truction operates must be v truction operated d 7. and PIC24E	ates in Word vord-aligned. ates in Byte r devices, this	mode, the so node, 'bit4' n instruction us	ource nust be ses the			
Words:	2: 3: 4:	When this ins register addre When this ins between 0 an In dsPIC33E DSRPAG regi	truction operates must be v truction operated d 7. and PIC24E	ates in Word vord-aligned. ates in Byte r devices, this	mode, the so node, 'bit4' n instruction us	ource nust be ses the			

**Note 1:** In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see **Note 3** in **Section 3.2.1 "Multi-Cycle Instructions"**.

Example 1:	BSET.B W3, #	#0x7	; Set bit 7	in W3
Example 2:	Before Instruction W3 0026 SR 0000 BSET [W4++],	W3 SR		
Data	Before Instruction W4 6700 6700 1734 SR 0000	lı W4 Data 6700 SR	After nstruction 6702 1735 0000	

BSW		Bit Write in	-				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F		
	Х	Х	X	Х	Х	Х	
Syntax:	{label:}	BSW.C	Ws,	Wb			
- ,		BSW.Z	[Ws],				
			[Ws++],				
			[Ws],				
			[++Ws],				
			[Ws],				
Operands:	Ws ∈ [W0 . Wb ∈ [W0 .						
Operation:	C →Ws< <u>For</u> ".Z" ope	For ".C" operation: C $\rightarrow$ Ws<(Wb)> For ".Z" operation (default): $\overline{Z} \rightarrow$ Ws<(Wb)>					
Status Affected:	Z →ws< None	(**6)-					
Encoding:	1010	1101	Zwww	w000	0ррр	SSSS	
	the destinat Wb, and eit The 'Z' bit s The 'w' bits The 'p' bits	nly the four Le ation bit numbe ither register d selects the C o s select the ad s select the sou s select the sou	er. Register d direct, or indire or Z flag as so ddress of the l ource Address	direct address rect addressin source. bit select regi s mode.	sing must be ng may be us	used for	
	Note:	This instruction	on only opera e ". Z" operatio	ates in Word ı		extension is	
Words:	1	provide_,	14 vp.		J.		
Cycles:	1 1 <sup>(1)</sup>						
read-mo details, s	C33E and PIC iodify-write ope , see <b>Note 3</b> in w.C w2, w3	erations on no 1 Section 3.2.2	on-CPU Specia 1 <b>"Multi-Cycl</b> ; Set b.	ial Function R	Registers. For ns".	r more	
W2 W3 SR	3 111F		After Instruction W2 7234 W3 111F		0)		

BSW.Z W2, W3 ; Set bit W3 in W2 to the complement Example 2: ; of the Z bit Before After Instruction Instruction E235 E234 W2 W2 W3 0550 W3 0550 SR 0002 (Z = 1, C = 0) SR 0002 (Z = 1, C = 0) Example 3: BSW.C [++W0], W6 ; Set bit W6 in [W0++] to the value ; of the C bit Before After Instruction Instruction W0 1000 W0 1002 W6 W6 34A3 34A3 Data 1002 Data 1002 2380 2388 SR 0001 (Z = 0, C = 1)SR 0001 | (Z = 0, C = 1)Example 4: BSW.Z [W1--], W5 ; Set bit W5 in [W1] to the ; complement of the Z bit ; Post-decrement W1 Before After Instruction Instruction W1 1000 W1 0FFE W5 888B W5 888B Data 1000 C4DD CCDD Data 1000 SR 0001 (C = 1) SR 0001 (C = 1)

BTG		Bit Toggle 1	i			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	
	Х	Х	Х	X	Х	Х
Syntax:	{label:}	BTG{.B}	f,	#bit4		
Operands:	f ∈ [0 81 bit4 ∈ [0 bit4 ∈ [0	191] for byte o 190] (even on 7] for byte o 15] for word	nly) for word opperation	operation		
Operation:	(f) <bit4> -</bit4>	→(f) <bit4></bit4>				
Status Affected:	None					
Encoding:	1010	1010	bbbf	ffff	ffff	fffb
Description:	operand, b advances t	file register 'f pit numbering to the Most S ation) of the b	begins with f Significant bit	the Least Sig	nificant bit (b	bit 0) and
		s select value s select the ad			ggle.	
	2:	rather than a denote a wor	a word operat rd operation, struction ope	nstruction der tion. You may , but it is not re erates in Word igned.	y use a .W ex required.	xtension to
			struction ope	erates in Byte	mode, 'bit4'	must be
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-mo details, s	Before	erations on no	on-CPU Speci <b>1 "Multi-Cyc</b> ; Toggle After	ial Function R	Registers. For ns".	
Data 1000 SR <u>Example 2:</u> BTG	R 0000	Data 100 Si 50, #0x8	R 0000	bit 8 in RA	AM660	
	Before Instruction	Data 1660	After Instruction			

Instruction Descriptions

BTG		Bit Toggle i	n Ws			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	BTG{.B}	Ws, [Ws],	#bit4		
			[Ws++],			
			[Ws],			
			[++Ws],			
			[Ws],			
Operands:		W15] 7] for byte op 15] for word				
Operation:	(Ws) <bit4></bit4>	→Ws <bit4></bit4>				
Status Affected:	None					
Encoding:	1010	0010	bbbb	0B00	0ppp	SSSS
	the Most S operations) The 'b' bits The 'B' bits The 's' bits	ing begins wit ignificant bit ( ). Register dir select value selects byte c select the so select the so	bit 7 for byte ect or indirec bit4, the bit p r word opera urce/destinat	operations, b t addressing osition to tes tion ('0' for w ion register.	hit 15 for word may be used t.	d I for Ws.
		The extension rather than a denote a wor	word operati	on. You may	use a .W ext	
		When this ins register addre				ource
		When this ins between 0 an	d 7.	-		
		In dsPIC33E DSRPAG reg Data Space.				
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-mo	odify-write op	24E devices, erations on no section 3.2.	on-CPU Spec	ial Function F	Registers. For	

Example 1:	BTG	W2, #	0×0	;	Toggle	bit O	in W2	
	I	Before		After				
	Ins	struction		Instruction				
	W2 F234		V	N2	F235			
	SR	0000		SR	0000			

Example 2: BTG	[W0++],	#0×0	; Toggle bit 0 ; Post-increme	
W0	Before nstruction 2300	W0	After nstruction 2302	
Data 2300	5606	Data 2300	5607	
SR	0000	SR	0000	

BTSC		Bit Test f,	Skip if Clear				
Implemented in	: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	BTSC{.B}	f,	#bit4			
Operands:	f ∈ [0 81 bit4 ∈ [0	191] for byte 190] (even o . 7] for byte . 15] for wor	nly) for word operation	operation			
Operation:	Test (f) <bit< td=""><td>4&gt;, skip if cl</td><td>ear</td><td></td><td></td><td></td></bit<>	4>, skip if cl	ear				
Status Affected	: None						
Encoding:	1010	1111	bbbf	ffff	ffff	fffb	
	and on the the next in the file reg begins with	Bit 'bit4' in the file register is tested. If the tested bit is '0', the next instruction (fetched during the current instruction execution) is discarded and on the next cycle, a NOP is executed instead. If the tested bit is '1', the next instruction is executed as normal. In either case, the contents of the file register are not changed. For the bit4 operand, bit numbering begins with the Least Significant bit (bit 0) and advances to the Most Significant bit (bit 7 for byte operations, bit 15 for word operations).					
		The 'b' bits select value bit4, the bit position to test. The 'f' bits select the address of the file register.					
		rather than a word operation. You may use a .W extension to denote a word operation, but it is not required.					
	3:		ist be word-ali nstruction ope	-	mode, 'bit4'	must be	
Words:	1	Detween O	anu 7.				
Cycles:	1 (2 or 3) <sup>(1</sup>	)					
reac deta	sPIC33E and PIC I-modify-write ope ails, see <b>Note 3</b> in	24E devices erations on r	ion-CPU Spec	ial Function F <b>:le Instructio</b>	Registers. Foi ns".	more	
Example 1:	002000 HERE: 002002 002004 002006 002008 BYPASS: 00200A	GOTO E  	0x1201, #2 3YPASS	; If bit ; skip th	2 of 0x120: e GOTO	1 is 0,	
Data 1	Before Instruction           PC         00 2000           200         264F           SR         00000	-	PC Data 1200 SR	After Instruction 00 2002 264F 0000			

01 01 01 01 01 01 01	02000 HERE: 02002 02004 02006 02008 BYPASS: 0200A	BTSC GOTO  	0x804, #1 BYPASS	,	t 14 of 0x804 the GOTO	is 0,
	Before			After		
	Instruction			Instruction		
F	PC 00 2000		PC	00 2006		
Data 080	04 2647		Data 0804	2647		
S	SR 0000		SR	0000		

BTSC			Bit Test W	s, Skip if Cle	ar		
Implemented	in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
		Х	Х	Х	Х	Х	Х
Syntax:		{label:}	BTSC	Ws,	#bit4		
				[Ws],			
				[Ws++],			
				[Ws],			
				[++Ws],			
				[Ws],			
Operands:		Ws ∈ [W0 bit4 ∈ [0					
Operation:		Test (Ws)<	bit4>, skip if	clear			
Status Affecte	ed:	None					
Encoding:		1010	0111	bbbb	0000	0ppp	SSSS
		register dire The 'b' bits The 'p' bits	ect or indired select value select the s	the Most Sign ct addressing bit4, the bit p cource Addres ource register	may be used position to tes s mode.	for Ws.	ora. Eitner
		Note:	This instruc	tion operates	in Word mod	e only.	
Words:		1				-	
Cycles:		1 (2 or 3 if 1	the next inst	truction is skip	ped) <sup>(1)</sup>		
re	ad-mod	lify-write ope	erations on n	s, the listed cy ion-CPU Spec 2.1 "Multi-Cyc	ial Function F	Registers. For	
Example 1:	0020 0020 0020	04 06 08 BYPASS:	GOTO  	W0, #0x0 BYPASS		bit 0 of W ip the GOTO	
		Before			After		
	PC	Instruction 00 2000	1	PC	Instruction 00 2002		
		00 2000	<u>-</u>		00 2002		

W0

SR

264F

0000

W0

SR

264F

00 00 00 00 00	02000 HERE: 02002 02004 02006 02008 BYPASS: 02008	BTSC GOTO  	W6, #0xF BYPASS	; If bit 15 of W6 is 0, ; skip the GOTO
Pi W Si	/6 264F		PC W6 SR	After Instruction 00 2006 264F 0000
00 00 00 00	03400 HERE: 03402 03404 03406 03408 BYPASS: 03408	BTSC GOTO  	[W6++], # BYPASS	OxC ; If bit 12 of [W6] is 0, ; skip the GOTO ; Post-increment W6
	Before Instruction			After Instruction
P	C 00 3400		PC	00 3402
W	6 1800		W6	1802
Data 180			Data 1800	1000
SI	R 0000		SR	0000

# 5

Instruction Descriptions

1		-	1		ī	
_	-	-			dsPIC33E	
Х	Х	Х	Х	Х	Х	
{label:}	BTSS{.B}	f,	#bit4			
f ∈ [0 8 bit4 ∈ [0	$f \in [0 \dots 8190]$ (even only) for word operation bit4 $\in [0 \dots 7]$ for byte operation					
Test (f) bi	t4>, skip if set					
None						
1010	1110	bbbf	ffff	ffff	fffb	
file registe with the Le bit (bit 7 fc The 'b' bits	r are not chan east Significan or byte operations s select value	ged. For the t bit (bit 0) ar on, bit 15 for bit4, the bit p	bit4 operand ad advances word operation osition to test	, bit numberin to the Most S on).	ng begins	
The 'f' bits	select the add	dress of the f	lle register.			
Note 1:	rather than a	word operation	on. You may	use a . W ext		
2:	2: When this instruction operates in Word mode, the file register					
3:	When this ins between 0 an	•	ates in Byte ı	mode, 'bit4' n	nust be	
1						
	{label:} f $\in$ [0 8: f $\in$ [0 8: bit4 $\in$ [0 bit4 $\in$ [0 Test (f) <bit None 1010 Bit 'bit4' in instruction and on the next instru file registe with the Le bit (bit 7 for The 'b' bits The 'f' bits Note 1: 2:</bit 	PIC24FPIC24HXX{label:}BTSS{.B} $f \in [0 \dots 8191]$ for byte of $f \in [0 \dots 8190]$ (even only bit4 $\in [0 \dots 7]$ for byte of bit4 $\in [0 \dots 15]$ for word Test (f) bit4>, skip if set None10101110Bit 'bit4' in the file register instruction (fetched duriny and on the next cycle, a next instruction is executifile register are not chan with the Least Significand bit (bit 7 for byte operation) The 'b' bits select value of The 'f' bits select the additionNote 1:The extension rather than a denote a word 2:When this inst address must	XXX{label:}BTSS{.B}f, $f \in [0 \dots 8191]$ for byte operation $f \in [0 \dots 8190]$ (even only) for word op $bit 4 \in [0 \dots 7]$ for byte operation $bit 4 \in [0 \dots 15]$ for word operation $bit 4 \in [0 \dots 15]$ for word operationTest (f) <bit 4="">, skip if setNone10101110bbfBit 'bit 4' in the file register 'f' is testedinstruction (fetched during the current and on the next cycle, a NOP is execut next instruction is executed as normal file register are not changed. For the with the Least Significant bit (bit 0) arbit (bit 7 for byte operation, bit 15 for the 'b' bits select value bit 4, the bit pThe 'b' bits select the address of the fileNote 1:The extension .B in the in rather than a word operation operation address must be word-aligned.</bit>	PIC24FPIC24HPIC24EdsPIC30FXXXXX{label:}BTSS{.B}f,#bit4f $\in$ [0 8191] for byte operationf $\in$ [0 8190] (even only) for word operationbit4 $\in$ [0 7] for byte operationbit4 $\in$ [0 7] for word operationbit4 $\in$ [0 15] for word operationTest (f) <bit4>, skip if setNone10101110bbbfffffBit 'bit4' in the file register 'f' is tested. If the testedinstruction (fetched during the current instruction eand on the next cycle, a NOP is executed instead. Inext instruction is executed as normal. In either cafile register are not changed. For the bit4 operandwith the Least Significant bit (bit 0) and advancesbit (bit 7 for byte operation, bit 15 for word operationThe 'b' bits select value bit4, the bit position to testThe 'b' bits select the address of the file register.Note 1:The extension .B in the instruction den rather than a word operation, but it is not re2:When this instruction operates in Word address must be word-aligned.</bit4>	PIC24FPIC24HPIC24EdsPIC30FdsPIC33FXXXXXX{label:}BTSS{.B}f,#bit4 $f \in [0 \dots 8191]$ for byte operationf (= [0 \ldots 8190] (even only) for word operationbit4 $\in [0 \dots 7]$ for byte operationbit4 $\in [0 \dots 15]$ for word operationbit4 $\in [0 \dots 15]$ for word operationTest (f) <bit4>, skip if setNone10101110bbbfbit 'bit4' in the file register 'f' is tested. If the tested bit is '1', the instruction (fetched during the current instruction execution) is and on the next cycle, a NOP is executed instead. If the tested bit next instruction is executed as normal. In either case, the contec file register are not changed. For the bit4 operand, bit numbering with the Least Significant bit (bit 0) and advances to the Most S bit (bit 7 for byte operation, bit 15 for word operation).The 'b' bits select value bit4, the bit position to test. The 'f' bits select the address of the file register.Note 1:The extension . B in the instruction denotes a byte or rather than a word operation, but it is not required.2:When this instruction operates in Word mode, the fil address must be word-aligned.</bit4>	

read-modify-write operations on non-CPU Special Function Regis details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1:	007100 HERE: 007102 007104	BTSS.B 0x1401, #0x1 ; If bit 1 of 0x1401 is 1, CLR WREG ; don't clear WREG 
Data	Before Instruction           PC         00 7100           1400         0280           SR         0000	After Instruction PC 00 7104 Data 1400 0280 SR 00000
Example 2:	007100 HERE: 007102 007104 007106 BYPASS:	BTSS 0x890, #0x9 ; If bit 9 of 0x890 is 1, GOTO BYPASS ; skip the GOTO 
Data	Before Instruction PC 00 7100 0890 00FE SR 0000	After Instruction PC 00 7102 Data 0890 00FE SR 0000

BTSS		Bit Test Ws	, Skip if Set			
Implemented in	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	BTSS	Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws],	#bit4		
Operands:	Ws ∈ [W0 . bit4 ∈ [0					
Operation:	Test (Ws)<	bit4>, skip if s	set.			
Status Affected:	None					
Encoding:	1010	0110	bbbb	0000	0ppp	SSSS
	cycle, a NO is executed For the bit4 (bit 0) and a	Bit 'bit4' in Ws is tested. If the tested bit is '1', the next instruction (fetche during the current instruction execution) is discarded and on the next cycle, a NOP is executed instead. If the tested bit is '0', the next instruction is executed as normal. In either case, the contents of Ws are not changed For the bit4 operand, bit numbering begins with the Least Significant bit (bit 0) and advances to the Most Significant bit (bit 15) of the word. Either register direct or indirect addressing may be used for Ws.				
	The 's' bits	select the va select the so select the so	urce register.		test.	
	Note:	This instruction	on operates i	in Word mode	e only.	
Words:	1					
Cycles:	1 (2 or 3 if 1	he next instru	uction is skip	ped) <sup>(1)</sup>		
read	PIC33E and PIC -modify-write ope ils, see <b>Note 3</b> in	erations on no	n-CPU Spec	ial Function F	Registers. For	
() () ()	002000 HERE: 002002 002004 002006 002008 BYPASS: 00200A		0, #0x0 YPASS		bit 0 of W p the GOTO	0 is 1,

0020	002	GOTO	BYPASS	; skip	the GOTO
0020	004				
0020	006				
0020	08 BYPASS:				
0020	00A				
	Before			After	
	Instruction			Instruction	
PC	00 2000		PC	00 2006	
W0	264F		W0	264F	
SR	0000		SR	0000	
·					

00 00 00 00 00	02000 HERE: 02002 02004 02006 02008 BYPASS: 0200A	BTSS GOTO  	W6, #0xF BYPASS	; If bit 15 of W6 is 1, ; skip the GOTO
	Before			After
	Instruction			Instruction
P	PC 00 2000		PC	00 2002
W	V6 264F		W6	264F
S	SR 0000		SR	0000
00 00 00 00	03400 HERE: 03402 03404 03406 03408 BYPASS: 0340A	BTSS GOTO  	[W6++], 0 BYPASS	xC ; If bit 12 of [W6] is 1, ; skip the GOTO ; Post-increment W6
	Before			After
	Instruction		_	Instruction
P	PC 00 3400		PC	00 3406
W	V6 1800		W6	1802
Data 180	00 1000		Data 1800	1000
S	SR 0000		SR	0000

### 5

Instruction Descriptions

BTST		Bit Test f					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	BTST{.B}	f,	#bit4			
Operands:	f ∈ [0 81 bit4 ∈ [0	91] for byte c 90] (even on 7] for byte o 15] for word	ly) for word operation	operation			
Operation:	(f) <bit4> →</bit4>	Z					
Status Affected:	Z						
Encoding:	1010	1011	bbbf	ffff	ffff	fffb	
	Bit 'bit4' in file register 'f' is tested and the complement of the tested bit is stored to the Z flag in the STATUS register. The contents of the file register are not changed. For the bit4 operand, bit numbering begins with the Least Significant bit (bit 0) and advances to the Most Significant bit (bit 7 for byte operation, bit 15 for word operation). The 'b' bits select value bit4, the bit position to be tested. The 'f' bits select the address of the file register.						
	2: 3:	rather than a denote a wor When this ins address mus	word operat d operation, struction ope t be word-ali struction ope	nstruction der ion. You may but it is not re rates in Word gned. rates in Byte	use a .Wex equired. I mode, the fi	tension to ile register	
Words:	1						
Cycles:	1 <sup>(1)</sup>						
read-mo details, s	dify-write ope	erations on no Section 3.2.	n-CPU Spec 1 "Multi-Cyc	cle count does ial Function R <b>le Instruction</b> = complement	Registers. For ns".		
			; bit 3	in 0x1201			
Data 120 Si		Data 12		(Z = 1)			
Example 2: BT	ST 0x13	02, #0x7		= compleme in 0x1302	nt of		
Data 130 S		Data 13 Z = 1)	After Instruction 02 F7FF SR 0000	I			

BTST Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
implemented in.	-	-	-				
	X	Х	X	Х	Х	Х	
Syntax:	{label:}	BTST.C	Ws,	#bit4			
		BTST.Z	[Ws],				
			[Ws++],				
			[Ws],				
			[++Ws],				
			[Ws],				
Operands:	Ws ∈ [W0 bit4 ∈ [0						
Operation:	(Ws) <bit For ".Z" op</bit 	$\frac{\text{For ".C" operation:}}{(Ws) < bit4> →C}$ $\frac{\text{For ".Z" operation (default):}}{(Ws) < bit4> →Z}$					
Status Affected:	Z or C						
Encoding:	1010	0011	bbbb	Z000	0ppp	SSSS	
Description:	specified, t STATUS re of the teste	register Ws is he compleme egister. If the " ed bit is stored contents of Ws	nt of the test . C" option of to the Carry	ed bit is store the instructio flag in the ST	d to the Zero n is specified	flag in the , the value	
For the bit4 operand, bit numbering begins with the Least Sigr (bit 0) and advances to the Most Significant bit (bit 15) of the v register direct or indirect addressing may be used for Ws. The 'b' bits select value bit4, the bit position to test. The 'Z' bit selects the C or Z flag as destination. The 'p' bits select the source Address mode. The 's' bits select the source register.							
	Note:	This instruction provided, the		ates in Word on is assume		extension is	
Words:	1						
Cycles:	1 <sup>(1)</sup>						

read-modify-write operations on non-CPU Special Function Registers. For more

details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

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Instruction Descriptions

Example 1:	BTST.C [W0++], #0x3	; Set C = bit 3 in [W0] ; Post-increment W0
Data 1	Before           Instruction           W0         1200           .200         FFF7           SR         0001	After Instruction W0 1202 1200 FFF7 SR 0000
Example 2:	BTST.Z W0, #0x7	; Set Z = complement of bit 7 in W0
	Before Instruction	After Instruction
	W0 F234	W0 F234
	SR 0000	SR 0002 (Z = 1)

BTST		Bit Test in \	1					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	BTST.C	Ws,	Wb				
		BTST.Z	[Ws],					
			[Ws++],					
			[Ws],					
			[++Ws],					
			[Ws],					
Operands:	$Ws \in [W0]$ $Wb \in [W0]$							
Operation:	(Ws)<(W For ".Z" op	$\frac{\text{For ".C" operation:}}{(Ws)<(Wb)> \rightarrow C}$ For ".Z" operation (default): (Ws)<(Wb)> →Z						
Status Affected:	Z or C							
Encoding:	1010	0101	Zwww	w000	0ppp	SSSS		
Description:	specified, t STATUS re complement	ht in register he value of the gister. If the ' nt of the teste either case, t	he tested bit is '. Z" option of d bit is stored	s stored to th the instruction to the Zero	e Carry flag i on is specifie flag in the ST	n the d, the		
	Only the four Least Significant bits of Wb are used to determine the bit number. Bit numbering begins with the Least Significant bit (bit 0) and advances to the Most Significant bit (bit 15) of the working register. Register direct or indirect addressing may be used for Ws.							
	The 'Z' bit selects the C or Z flag as destination. The 'w' bits select the address of the bit select register. The 'p' bits select the source Address mode. The 's' bits select the source register.							
	Note:	This instructi provided, the		ates in Word on is assume		extension i		
Words:	1							
Cycles:	1(1)							

**Note 1:** In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see **Note 3** in **Section 3.2.1 "Multi-Cycle Instructions"**.

Example 1: BTST

BTST.C W2, W3

; Set C = bit W3 of W2

W W SI	3 2368	After Instruction W2 F234 W3 2368 SR 0000	
Example 2: BT	ſST.Z [₩0++], ₩1	; Set Z = complemer ; bit W1 in [W0], ; Post-increment W0	
	Before	After	
	Instruction	Instruction	
W	/0 1200	W0 1202	
W	/1 CCC0	W1 CCC0	
Data 120	00 6243 C	oata 1200 6243	
S	R 0002 (Z = 1)	SR 0000	

BTSTS		Bit Test/Set	f					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	BTSTS{.B}	f,	#bit4				
Operands:	f ∈ [0 81 bit4 ∈ [0	$f \in [0 \dots 8191]$ for byte operation $f \in [0 \dots 8190]$ (even only) for word operation $bit 4 \in [0 \dots 7]$ for byte operation $bit 4 \in [0 \dots 15]$ for word operation						
Operation:	(f) <bit4> → 1 →(f)<bit4< td=""><td></td><td></td><td></td><td></td><td></td></bit4<></bit4>							
Status Affected:	Z							
Encoding:	1010	1100	bbbf	ffff	ffff	fffb		
Description:	Bit 'bit4' in file register 'f' is tested and the complement of the tested be stored to the Zero flag in the STATUS register. The tested bit is then to '1' in the file register. For the bit4 operand, bit numbering begins w the Least Significant bit (bit 0) and advances to the Most Significant (bit 7 for byte operations, bit 15 for word operations).							
	The 'b' bits select value bit4, the bit position to test/set. The 'f' bits select the address of the file register.							
	<b>Note 1:</b> The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a . W extension to denote a word operation, but it is not required.							
		When this ins address mus			d mode, the f	ïle register		
	3:	When this ins between 0 ar	struction ope	-	mode, 'bit4'	must be		
	4:	The file regis	ter 'f' must n	ot be the CP	U Status reg	ister (SR).		
Words:	1							
Cycles:	1 <sup>(1)</sup>							

**Note 1:** In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see **Note 3** in **Section 3.2.1 "Multi-Cycle Instructions"**.

Example 1: BTSTS.B 0x1201, #0x3 ; Set Z = complement of bit 3 in 0x1201, ; then set bit 3 of 0x1201 = 1 Before After Instruction Instruction Data 1200 F7FF Data 1200 FFFF SR 0000 SR 0002 (Z = 1) ; Set Z = complement of bit 15 in 0x808, Example 2: BTSTS 0x808, #15 ; then set bit 15 of 0x808 = 1 Before After

I	ו ו	nstruction	
RAM300	8050	RAM300	8050
SR	0002	(Z = 1) SR	0000

BTSTS		Bit Test/Se	t in Ws							
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E				
	Х	Х	Х	Х	Х	Х				
Syntax:	{label:}	BTSTS.C	Ws,	#bit4						
		BTSTS.Z	[Ws],							
			[Ws++],							
			[Ws],							
			[++Ws],							
			[Ws],							
Operands:	Ws ∈ [W0 bit4 ∈ [0									
Operation:	<u>For ".C" op</u> (Ws) <bit< td=""><td>t4&gt; →C</td><td></td><td></td><td></td><td></td></bit<>	t4> →C								
		$1 \rightarrow Ws < bit 4 >$								
		$\frac{\text{For ".Z" operation (default):}}{\text{(Ws)}} \rightarrow Z$								
	(1)→Ws<									
Status Affected:	Z or C									
Encoding:	1010	0100	bbbb	Z000	0ppp	SSSS				
Description:	specified, t STATUS re of the teste	ent of the test '.C" option of	e".Z" option ed bit is store the instructio flag in the S L'.	d to the Zerc n is specified	flag in the I, the value					
		The 'b' bits select the value bit4, the bit position to test/set.								
		The 'Z' bit selects the C or Z flag as destination. The 'p' bits select the source Address mode.								
	•	select the so								
				ates in Word r on is assume		xtension is				
		If Ws is used CPU Status r	•	it must not co	ntain the add	ress of the				
				devices, this ect address g						
	1									
Words:	-									

details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1: BTSTS.C [W0++], #0x3	; Set C = bit 3 in [W0] ; Set bit 3 in [W0] = 1 ; Post-increment W0
Before	After
Instruction	Instruction
W0 1200	W0 1202
Data 1200 FFF7 Data	1200 FFFF
SR 0001 (C = 1)	SR 0000
Example 2: BTSTS.Z W0, #0x7	; Set Z = complement of bit 7 ; in W0, and set bit 7 in W0 = 1
Before	After
Instruction	Instruction
W0 F234 SR 0000	W0 F2BC SR 0002 (Z = 1)

CALL			Call Subrou	utine			
Implemented in	n:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
		Х	Х		Х	Х	
Syntax:		{label:}	CALL	Expr			
Operands:			e a label or e				86061.
Operation:		Expr is resolved by the linker to a lit23, where lit23 $\in$ [0 8388606]. (PC) + 4 $\rightarrow$ PC (PC<15:0>) $\rightarrow$ (TOS) (W15) + 2 $\rightarrow$ W15 (PC<23:16>) $\rightarrow$ (TOS) (W15) + 2 $\rightarrow$ W15 lit23 $\rightarrow$ PC NOP $\rightarrow$ Instruction Register					
Status Affected	d:	None	0				
Encoding:			1	1	1	1	
1st word		0000	0010	nnnn	nnnn	nnnn	nnn0
2nd word Description:		0000	0000	0000	0000	0nnn	nnnn
Description: Direct subroutine call over the entire 4-Mbyte instruction program memory range. Before the CALL is made, the 24-bit return address (PC + 4) is PUSHed onto the stack. After the return address is stacked, the 23-bit value 'lit23' is loaded into the PC. The 'n' bits form the target address.						address	
			The linker wi be used.	ill resolve the	e specified ex	opression into	o the lit23 to
Words:		2					
Cycles:		2					
Example 1:	0260 0260	04	CALL _FI MOV W0, 	IR W1	; Cal	ll _FIR sub	routine
	0268 0268	44 _FIR: 46	MOV #0x4	400, W2	; _FI	IR subrouti	ne start
		Before			After		
	r	Instruction	-		nstruction		
	PC	02 6000		PC	02 6844		
	W15	A268		W15	A26C		
Data A	-	FFFF		ata A268	6004		
Data A	-	FFFF		ata A26A	0002		
	SR	0000	)	SR	0000		

Example 2: 0720 0720			G66 0, W1	; call ro	utine _G66	
077/ 077/ 077/		 INC W	6, [W7++]	; routine	start	
PC W15 Data 9004 Data 9006 SR	Before Instruction 07 2000 9004 FFFF FFFF 00000		PC W15 Data 9004 Data 9006 SR	After nstruction 07 7A28 9008 2004 0007 0000		
CALL		Call Subrou	utine			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
Syntax: Operands: Operation:	$\begin{array}{                                    $					
Status Affected: Encoding:	0 →SFA bit lit23 →PC NOP →Instr SFA	uction Regist	er			
1st word	0000	0010	nnnn	nnnn	nnnn	nnn0
2nd word Description:	0000000000000nnnnnnnDirect subroutine call over the entire 4-Mbyte instruction program memory range. Before the CALL is made, the 24-bit return address (PC + 4) is PUSHed onto the stack. After the return address is stacked, the 23-bit value 'lit23' is loaded into the PC.The 'n' bits form the target address.					
	Note:	The linker wi		e specified ex	pression into	o the lit23 to
Words: Cycles:	2 4	be used.	-			

0260	xample 1: 026000 026004		_FIR W0, W1	; Call _FIR subroutine			
0268 0268	344 _FIR: 346	 MOV	#0x400, W2	; _FIR subroutine start			
Before Instruction				After Instruction			
PC	02 6000		PC	02 6844			
W15	A268		W15	A26C			
Data A268	FFFF		Data A268	6004			
Data A26A	FFFF		Data A26A	0002			
SR	0000		SR	0000			
Example 2: 072000 072004		CALL MOV	_G66 W0, W1	; call routine _G66			
077A28 _G66: 077A2A 077A2C		INC	W6, [W7++]	] ; routine start			
Before				After			
Instruction			Instruction				
PC	07 2000	]	PC	07 7A28			
W15	9004		W15	9008			
Data 9004	FFFF		Data 9004	2004			
Data 9006	FFFF		Data 9006	0007			
SR	0000	]	SR	0000			

				deDICOOF	deDICOOF	deDICOCC
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	X	Х		Х	Х	
Syntax:	{label:}	CALL	Wn			
Operands:	Wn∈ [W0	W15]				
Operation:		) →TOS →W15 >) →TOS →W15				
Status Affected:	None					
Encoding:	0000	0001	0000	0000	0000	SSSS
Description:		routine call o		32K instructio	ns of prograi	m memory
Description:	Before the onto the sta into PC<15 Wn<0> is iq	CALL is made ack. After the :1> and PC< gnored.	e, the 24-bit r return addre: 22:16> is clea	32K instructio eturn addres ss is stacked ared. Since P	ns of program s (PC + 2) is , Wn<15:1> i	m memory. PUSHed is loaded
	Before the onto the sta into PC<15 Wn<0> is ig The 's' bits	CALL is made ack. After the :1> and PC<	e, the 24-bit r return addre: 22:16> is clea	32K instructio eturn addres ss is stacked ared. Since P	ns of program s (PC + 2) is , Wn<15:1> i	m memory PUSHed is loaded
Description: Words: Cycles:	Before the onto the sta into PC<15 Wn<0> is iq	CALL is made ack. After the :1> and PC< gnored.	e, the 24-bit r return addre: 22:16> is clea	32K instructio eturn addres ss is stacked ared. Since P	ns of program s (PC + 2) is , Wn<15:1> i	m memory. PUSHed is loaded
Words:	Before the onto the sta into PC<15 Wn<0> is ig The 's' bits 1 2	CALL is made ack. After the :1> and PC< gnored.	e, the 24-bit r return addre: 22:16> is clea urce register. ;	32K instructio eturn addres ss is stacked ared. Since P	ns of prograi s (PC + 2) is , Wn<15:1> i 2C<0> is alwa	m memory PUSHed is loaded ays '0',
Words: Cycles: <u>Example 1:</u> 0010 0010	Before the onto the sta into PC<15 Wn<0> is ig The 's' bits 1 2 02 04 00 _B00T:	CALL is made ack. After the :1> and PC<: gnored. select the so CALL W0	e, the 24-bit r return addre: 22:16> is clea urce register. ; ;	32K instructio eturn addres ss is stacked ared. Since F Call BOOT s	ns of program s (PC + 2) is , Wn<15:1> i PC<0> is alway ubroutine i	m memory PUSHed is loaded ays '0',
Words: Cycles: <u>Example 1:</u> 0010 0010 0016	Before the onto the sta into PC<15 Wn<0> is ig The 's' bits 1 2 02 04 00 _B00T:	CALL is made ack. After the :1> and PC<: gnored. select the sol  MOV #0x400, 	e, the 24-bit r return addre 22:16> is clea urce register. ; ; W2 ; W6	32K instructio eturn addres ss is stacked ared. Since F Call BOOT s using W0	ns of program s (PC + 2) is , Wn<15:1> i PC<0> is alway ubroutine i	m memory PUSHed is loaded ays '0',
Example 2: 00420 00420		CALL W7		all TEST su sing W7	broutine ir	directly
---	---	---	----------------------------------	---	-------------------------------	--------------------
0055( 0055)	00 _TEST: 02	INC W1, W DEC W1, W		TEST starts	here	
PC W7 W15 Data 6F00 Data 6F02 SR	Before Instruction 00 4200 5500 6F00 FFFF FFFF 0000		PC	After struction 00 5500 5500 6F04 4202 0000 0000		
CALL		Call Indirect	t Subroutine	2		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	CALL	Wn			
Operands:	Wn∈ [W0	W15]				
Operation:	(W15) + 2 - (PC<23:16) (W15) + 2 - 0 →SFA bit 0 →PC<22 (Wn<15:1>	) →TOS, SFA →W15 >) →TOS →W15		>		
Status Affected:	SFA					
Encoding:	0000	0001	0000	0000	0000	SSSS
Description:	Before the onto the sta	oroutine call o CALL is made ack. After the ::1> and PC<2 gnored.	e, the 24-bit r return addre:	eturn addres ss is stacked	s (PC + 2) is , Wn<15:1> i	PUSHed s loaded
	The 's' bits	select the so	urce register.			
Words:	1					
Cycles:	4					

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CALL.L		Call Indirec	t Subroutin	e Long		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	CALL.L	Wn			
Operands:	Wn∈ [W0,	W2, W4, W6	, W8, W10, <sup>v</sup>	W12]		
Operation:	$(PC) +2 \rightarrow F$ $(PC<15:1>)$ $(W15)+2 \rightarrow$ $(PC<23:16:2)$ $(W15)+2 \rightarrow$ $0 \rightarrow SFA bit$ $PC<23> \rightarrow F$ $PC<15:0>$	PC, ) →TOS<15:1 W15 >) →TOS, W15 , PC<23> (see	L>, SFA bit – text); (Wn+:	→TOS<0>	c<22:16>; (W	′n) →
		ruction Regis	ter			
Status Affected:	SFA	0004				
Encoding: Description:	0000	0001 proutine call to	1www	w000	0000	SSSS
	pushed onto Then, the L value (Wn) PC<23> is in The content The value of The 's' bits	C+2) and the o the system S 7-bits of (V is loaded into not modified ts of (Wn+1)- of Wn<0> is a specify the a specify the a	stack, after Vn+1) are loa PC<15:0>. by this instru <15:7> are ig Ilso ignored ddress of the	which the SF aded in PC<2 Inction. gnored. and PC<0> is e Wn source	A bit is clear 22:16>, and t s always set register.	ed. he 16-bit
Words:	1					
Cycles:	4					
Example 1: 0260 0260		CALL.L W4 MOV W0, 	Wl	; Cal	l_FIR sub	routine
0268 0268	44 _FIR: 46	MOV #0x4	100, W2	; _FI	R subrouti	ne start
	Before			After		
-	Instruction	_	<u> </u>	nstruction		
PC	02 6000		PC	02 6844		
W4	6844		W4	6844		
W5	0002		W5	0002		
W15	A268		W15	A26C		
Data A268	FFFF	_	ata A268	6004		
Data A26A	FFFF	_	ata A26A	0002		
SR	0000	<u></u>	SR	0000		

CLR		Clear f or W	REG			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	CLR{.B}	f			
			WREG			
Operands:	f∈ [0 81	91]				
Operation:	0 →destina	tion designat	ed by D			
Status Affected:	None					
Encoding:	1110	1111	0BDf	ffff	ffff	ffff
Description:		ontents of a fi specified, the s cleared.				
	The 'D' bit	selects byte o selects the de select the ado	stination ('0'	for WREG, "		
		The extensior rather than a denote a wore	word operati	on. You may	use a .W ext	
	2:	The WREG is	set to worki	ng register W	/0.	
Words:	1					
Cycles: Example 1: CL	1 R.B RAM20	0; C	lear RAM200	0 (Byte mod	e)	
RAM200 SF		RAM20 SF				
Example 2: C	LR WREG	; (	Clear WREG	(Word mode	)	
WRE( SI		WRE S				

CLR		Clear Wd				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	CLR{.B}	Wd			
			[Wd]			
			[Wd++]			
			[Wd]			
			[++Wd]			
			[Wd]			
Operands:	Wd ∈ [W0	W15]				
Operation:	$0 \rightarrow Wd$					
Status Affected:	None					
Encoding:	1110	1011	0Bqq	qddd	d000	0000
Description:		contents of reg may be used		her register d	lirect or indire	ect
	The 'q' bits	select byte or select the de select the de	estination Add	dress mode.	ord, '1' for by	ie).
	Note:	The extensio rather than a	on . B in the	instruction de tion. You may but it is not re	y use a .W e	
Words:	1		-		·	
Cycles:	1					
Example 1:	CLR.B W2	; Cl	Lear W2 (Byt	te mode)		
	Before		After			
	Instruction					
	W2 3333 SR 0000		V2 3300 SR 0000			
Example 2:	CLR [W0+		Lear [W0] ost-incremer	nt WO		
Data 2	Before Instruction W0 2300 2300 5607 SR 0000	W Data 230	After Instruction V0 2302 00 0000 SR 0000			

CLR		Clear Acc	cumulator, Pi	refetch Oper	ands		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
				Х	Х	Х	
Syntax: {label:}	CLR	Acc	{,[Wx],Wxd}	{,[Wy]	,Wyd}	{,AWB}	
	$\{,[Wx] + = kx,Wxd\} \{,[Wy] + = ky,Wyd\}$						
			{,[Wx] – = kx	,Wxd} {,[Wy]	<pre>- = ky,Wyd}</pre>		
			{,[W9 + W12]	],Wxd} {,[W11	. + W12],Wyd]	ł	
Operands:		W9]; kx ∈ ), W11]; ky	[-6, -4, -2, 2, ∈ [-6, -4, -2, + = 2]			]	
Operation:	$0 \rightarrow Acc(A \text{ or } B)$ $([Wx]) \rightarrow Wxd; (Wx) +/- kx \rightarrow Wx$ $([Wy]) \rightarrow Wyd; (Wy) +/- ky \rightarrow Wy$ $(Acc(B \text{ or } A)) \text{ rounded } \rightarrow AWB$						
Status Affected:	OA, OB, SA	A, SB					
Encoding:	1100	0011	A0xx	yyii	iijj	jjaa	
Description:	operands in the non-sp	n preparati ecified acc	e specified acc on for a MAC t umulator resu nd saturate fla	ype instructio Ilts. This instr	on and optionation of the second s	ally store the	
	which supp Section 4.2 register dire	oort indirect 14.1 "MAC ect or indire	Wy and Wyd s t and register <b>Prefetches</b> " ect store of th or, as describ	offset addres . Operand AV e convergent	sing, as desc VB specifies t ly rounded co	ribed in he optional ontents of	
	The 'x' bits The 'y' bits The 'i' bits The 'j' bits	select the select the select the select the v	other accumu prefetch Wxd prefetch Wyd Wx prefetch o Wy prefetch o accumulator	destination. destination. peration. peration.			
Words:	1						
Cycles:	1						

; Load W4 with [W8], post-inc W8

; Clear ACCA

		; Stor	e ACCB to W13	
	Before Instruction		After Instruction	
W4	F001	W4	1221	1
W8	2000	W8	2002	
W13	C623	W13	5420	
ACCA	00 0067 2345	ACCA	00 0000 0000	
ACCB	00 5420 3BDD	ACCB	00 5420 3BDD	
Data 2000	1221	Data 2000	1221	
SR	0000	SR	0000	
Example 2: CLR	B, [W8]+=2, W6,	[W10]+=2, W7,	,	Clear A

CLR A, [W8]+=2, W4, W13

Example 1:

; Clear ACCB ; Load W6 with [W8] ; Load W7 with [W10] ; Save ACCA to [W13] ; Post-inc W8,W10,W13

	Before Instruction		After Instruction
W6	F001	W6	1221
W7	C783	W7	FF80
W8	2000	W8	2002
W10	3000	W10	3002
W13	4000	W13	4002
ACCA	00 0067 2345	ACCA	00 0067 2345
ACCB	00 5420 ABDD	ACCB	00 0000 0000
Data 2000	1221	Data 2000	1221
Data 3000	FF80	Data 3000	FF80
Data 4000	FFC3	Data 4000	0067
SR	0000	SR	0000

-

CLRWDT	-	Clear Watch	ndog Timer			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	CLRWDT				
Operands:	None					
Operation:	0 →WDT p	ount register rescaler A co rescaler B co				
Status Affected:	None					
Encoding:	1111	1110	0110	0000	0000	0000
Description:	prescaler c	ontents of the ount registers	s. The Watcl	ndog Prescal	er A and Pre	scaler B
Words:	1					
Cycles:	1					
Example 1:	CLRWDT ;	Clear Watc	hdog Timer			
	Before Instruction SR 0000	SI	After Instruction R 0000			

# **Section 5. Instruction Descriptions**

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	COM{.B}	f	{,WREG}		
Operands:	f∈ [0 81	91]				
Operation:	(f) →destin	ation designa	ted by D			
Status Affected:	N, Z					
Encoding:	1110	1110	1BDf	ffff	ffff	ffff
	stored in V register. The 'B' bit The 'D' bit	the destinat VREG. If WRE selects byte o selects the de select the add	EG is not spo or word opera estination ('0'	ecified, the re tion ('0' for w for WREG, '2	esult is store ord, '1' for b	d in the file yte).
		The extension rather than a denote a word The WREG is	word operati d operation, l	on. You may but it is not re	use a .W ext quired.	
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-mo	dify-write op	24E devices, erations on no section 3.2.	on-CPU Spec	ial Function F	Registers. For	
Example 1: 0	COM.b RAM2	:00 ; COM	RAM200 (B	yte mode)		
	Before					
RAM20 S	Instruction 00 80FF SR 0000	RAM20		(Z)		
S	00 80FF SR 0000	RAM20	Instruction 00 8000 6R 0002	1400 and sto	ore to WREG	i

COM		Compleme	nt Ws			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	COM{.B}	Ws,	Wd		
-			[Ws],	[Wd]		
			[Ws++],	[Wd++]		
			- [Ws],	[Wd]		
			[++Ws],	[++Wd]		
			[Ws],	[Wd]		
Operands:	Ws ∈ [W0 Wd ∈ [W0					
Operation:	(Ws) →Wd					
Status Affected:	N, Z					
Encoding:	1110	1010	1Bqq	qddd	dppp	SSSS
	The 'q' bits The 'd' bits The 'p' bits	selects byte c select the de select the de select the so select the so	estination Add estination reg ource Addres	dress mode. ister. s mode.	rord, '1' for by	/te).
	Note:	rather than a	a word opera	instruction de tion. You may	yusea.We	
Words:	1	denote a wor	u operation,	but it is not re	equireu.	
Cycles:	1 1 <sup>(1)</sup>					
read-mo	dify-write op see <b>Note 3</b> ir	C24E devices, erations on no section 3.2. [W1++]	on-CPU Spec <b>1 "Multi-Cyc</b> ; COM [W0]	ial Function F	Registers. For <b>ns"</b> . to [W1] (By	more
ا W0 W1 Data 2300 Data 2400 SR	Before nstruction 2301 2400 5607 ABCD 0000	V Data 23 Data 24	After Instruction V0 2302 V1 2401 00 5607			

Example 2: COM	W0, [W1++		OM WO and s ost-increme	-	1] (Word mo	de)
	Before struction D004 1000 ABA9 0000	W( W2 Data 100( SF	1 1002 0 2FFB			
СР		Compare f v	vith WREG,	Set Status F	lags	
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	CP{.B}	f			
Operands:	f∈ [0819	91]				
Operation:	(f) – (WRE0	G)				
Status Affected:	DC, N, OV,	Z, C				
Encoding:	1110	0011	0B0f	ffff	ffff	ffff
Description:	is equivaler not stored. The 'B' bit s	) – (WREG) a nt to the SUBW selects byte o select the add	IF instruction	, but the resu tion ('0' for w	ult of the subt	raction is
	Note 1:	The extensior rather than a denote a word The WREG is	n . B in the in word operation, I d operation, I	struction den on. You may out it is not re	use a .W exte equired.	
Words:	1					
Cycles:	1(1)					
read-mo	dify-write ope ee <b>Note 3</b> in	24E devices, erations on no Section 3.2. 90 ; Comp	n-CPU Spec 1 "Multi-Cyc	ial Function F I <mark>e Instructio</mark>	Registers. For	more
WREG RAM400 SF <u>Example 2:</u> CP	0 0823		00 0823 SR 0003	(C = 1)	EG (Word mo	de)
WREG Data 1200 SF	2277	WRE Data 12		(N = 1)		

CP		Compare Wb with lit5, Set Status Flags					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х		Х	Х		
Syntax:	{label:}	CP{.B}	Wb,	#lit5			
Operands:	Wb ∈ [W0 lit5 ∈ [ 0 .						
Operation:	(Wb) – lit5						
Status Affected:	DC, N, OV	, Z, C					
Encoding:	1110	0001	0www	wB00	011k	kkkk	
Description:	equivalent	Wb) – lit5, and to the SUB ins gister direct a	struction, but	the result of	the subtraction		
	The 'B' bit	s select the ac selects byte o provide the li	r word opera	tion ('0' for w	ord, '1' for by		
	Note:	The extension rather than a denote a wor	word opera	tion. You may	y use a .W e		
Words:	1						
Cycles:	1						
Example 1:	CP.B W4, #0	x12 ;	Compare W4	with 0x12	(Byte mode	)	
	Before Instruction W4 7711 SR 0000	W		N = 1)			
Example 2:	CP W4, #0	x12 ;	Compare W4	with 0x12	(Word mode	)	
	Before Instruction W4 7713 SR 0000	-	After Instruction V4 7713 SR 0001	(C = 1)			

СР		Compare W	b with lit8, S	Set Status Fl	ags	
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	CP{.B}	Wb,	#lit8		
Operands:	Wb ∈ [W0 lit8 ∈ [ 0 .					
Operation:	(Wb) – lit8					
Status Affected:	DC, N, OV	, Z, C				
Encoding:	1110	0001	0www	wBkk	k11k	kkkk
Description:	equivalent	Wb) – lit8, and to the SUB ins gister direct a	struction, but	the result of	the subtraction	
	The 'B' bit	s select the ac selects byte o provide the li	or word opera	tion ('0' for w	ord, '1' for b	
	Note:	The extension rather than a denote a wor	word opera	tion. You may	yuse a.We	
Words:	1					
Cycles:	1					
Example 1:	CP.B W4, #0	x12 ;	Compare W4	with 0x12	(Byte mode	)
	Before Instruction W4 7711 SR 0000	W. Sł		N, C = 1)		
Example 2:	CP W4, #0	x12 ;	Compare W4	with 0x12	(Word mode	)
	Before Instruction W4 7713 SR 0000	-	After Instruction V4 7713 SR 0001	) (C = 1)		

CP		Compare W	/b with Ws, S	Set Status Fla	ags	
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	CP{.B}	Wb,	Ws		
2			·	[Ws]		
				[Ws++]		
				[Ws]		
				[++Ws]		
				[Ws]		
Operands:	Wb∈ [W0 Ws∈ [W0					
Operation:	(Wb) – (Ws	6)				
Status Affected:	DC, N, OV,	Z, C				
Encoding:	1110	0001	0www	wB00	0ppp	SSSS
	The 'B' bit The 'p' bits	selects byte c select the so	or word opera urce Address	Wb source re ation ('0' for wo s mode. Ws source reg	ord, '1' for by	te).
	Note:	The extension rather than a	on .B in the word opera	instruction de tion. You may	enotes a byt / use a .W e	
Mordo	1	denote a wor	a operation,	but it is not re	quirea.	
Words: Cycles:	1 1 <sup>(1)</sup>					
read-m details,	odify-write op	oerations on n n <b>Section 3.2</b> /1++] ; (	on-CPU Spe 2.1 "Multi-Cy	rcle count doe cial Function F <b>cle Instructio</b> ] with W0 (I ent W1	Registers. Foi ns".	
	Before	, .	After			
V	Instruction V0 ABA9 V1 2000		Instructio W0 ABA9 W1 2001	n ] -		
Data 200 S	00 D004 SR 0000	Data 20	000 D004 SR 0009	(N, C = 1)		

Example 2:	СР	W5,
------------	----	-----

Before Instruction					
W5	2334				
W6	8001				
SR	0000				

W6

; Compare W6 with W5 (Word mode)

	After						
Instruction							
W5	2334						
W6	8001						
SR	000C	(N, OV = 1)					

CP0		Compare f v	vith 0x0, Set	Status Flag	S	
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	CP0{.B}	f			
Operands:	f∈ [0 81	91]				
Operation:	(f) – 0x0					
Status Affected:	DC, N, OV,	Z, C				
Encoding:	1110	0010	0B0f	ffff	ffff	ffff
Description:		) – 0x0 and u is not stored.	•	ATUS registe	r. The result	of the
		selects byte o select the add			ord, '1' for by	/te).
		The extensio rather than a denote a wor	word operat	ion. You may	/usea.We	
Words:	1		•		•	
Cycles:	1 <sup>(1)</sup>					
read-m details, <u>Example 1:</u> C RAM1	C33E and PIC odify-write op see <b>Note 3</b> in P0.B RAM Before Instruction 00 44C3 SR 0000	erations on no Section 3.2. 100 ; Co RAM1	n-CPU Spec 1 "Multi-Cyc mpare RAM10 After Instruction	ial Function F l <mark>e Instructio</mark> 00 with 0x0	Registers. Foi ns".	more
Example 2: CF	P0 0x1FFE	; Compai	re (0x1FFE)	with 0x0 (	Word mode)	
Data 1FF	Before Instruction E 0001 R 0000	Data 1Fl	After Instruction =E 0001 SR 0001	(C = 1)		

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
•	X	X	X	X	X	X
Syntax:	{label:}	CP0{.B}	Ws			
	l	<b>G</b> . (	[Ws]			
			[WS] [WS++]			
			[Ws]			
			[++Ws]			
			[Ws]			
Operands:	Ws∈ [W0	W15]				
Operation:	(Ws) – 0x0	-				
Status Affected:	DC, N, OV,					
Encoding:	1110	0000	0000	0B00	0ррр	SSSS
Description:	Compute (\	(Ws) – 0x0000 ction is not sto /s.	) and update	the STATUS	register. The	e result of
	The 'p' bits	selects byte o s select the so s select the add	ource Address	s mode.		yte).
		rather than a	on . B in the i a word operat rd operation, l	tion. You may	y use a .W e	
Words:	1					
Cycles:	1(1)					
read-mo details, s	odify-write ope		on-CPU Speci	ial Function R cle Instruction with 0 (Byte	Registers. For ons".	
	Before		After			
	Instruction	,		í		
	4 1001	V	N4 1000			
W <sup>2</sup> Data 1000			0034			
W4 Data 1000 SF	0 0034	Data 100		(C = 1)		
Data 1000	0 0034 R 0000	Data 100 S			)rd mode)	

CPB	Compare f with WREG using Borrow, Set Status Flags						
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	CPB{.B}	f				
Operands:	f∈ [081	91]					
Operation:	(f) – (WRE	G) – ( <del>C</del> )					
Status Affected:	DC, N, OV	Z, C					
Encoding:	1110	0011	1B0f	ffff	ffff	ffff	
Description:	instruction subtraction The 'B' bit	f) – (WREG) - is equivalent is not stored selects byte o select the add	to the SUBB i or word opera	nstruction, bu tion ('0' for w	ut the result of	of the	
		rather than a word operation. You may use a .W extension to denote a word operation, but it is not required.					
	2.	The WREG is	s sat ta warki	M ratistar M	/∩		
	3:	The WREG is The Z flag is ' These instruc	'sticky" for Al	DDC, CPB,		JBBR.	
Words:	3:	The Z flag is '	'sticky" for Al	DDC, CPB,		JBBR.	

read-modify-write operations on non-CPU Special Function Registers. For more details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1: CPB.B RAM400 ; Compare RAM400 with WREG using C (Byte mode)

I	Before nstruction	l	After nstructior	ı
WREG	8823	WREG	8823	
RAM400	0823	RAM400	0823	
SR	0000	SR	0008	(N = 1)

СРВ 0x1200 ; Compare (0x1200) with WREG using C (Word mode) Example 2:

		After				
I	nstructior	Instruction				
WREG	2377		WREG	2377		
Data 1200	2377	Da	ata 1200	2377		
SR	0001	(C = 1)	SR	0001	(C = 1)	

СРВ	Compare \	Nb with lit5 ເ	using Borrov	<i>w</i> , Set Status	Flags	
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
-	Х	Х		Х	Х	
Syntax:	{label:}	CPB{.B}	Wb,	#lit5		
Operands:	Wb ∈ [W0 lit5 ∈ [ 0					
Operation:	(Wb) – lit5	-				
Status Affected:	DC, N, OV,					
Encoding:	1110	0001	1www	wB00	011k	kkkk
Description:	instruction	is equivalent	to the SUBB i	e the STATU nstruction, bu ect addressin	it the result o	of the
	The 'B' bit s	selects byte o	r word opera	Wb source re tion ('0' for w d, a five bit int	ord, '1' for by	
	2:	rather than a denote a wore The Z flag is "	word operati d operation, l sticky" for AD	struction deno on. You may i but it is not re DDC, CPB, S	use a .W exte quired.	ension to
Marda.		instructions c	an only clear	Ζ.		
Words: Cycles:	1 1					
Example 1: CPF		v	After Instruction V4 7711	ith 0x12 us (N=1)	ing C (Byte	: mode)
Example 2: CPB	.B W4, #0	<12 ; Cor	mpare W4 wi	th 0x12 usi.	.ng C (Byte	mode)
W4 SR		W		(N = 1)		
Example 3: CPB	W12, #0	€x1F ; Co	mpare W12 w	/ith 0x1F us	ing C (Word	d mode)
W12 SR Example 4: CPB	0002 (Z		R 0003 (	(Z,C=1) ith 0x1F us	ing C (Word	1 mode)
	Before	W1	After Instruction 2 0020	C = 1)	ing o (word	, mode)

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СРВ	Compare Wb with lit8 using Borrow, Set Status Flags						
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
			Х			Х	
Syntax:	{label:}	CPB{.B}	Wb,	#lit8			
Operands:	Wb ∈ [W0 lit8 ∈ [ 0						
Operation:	(Wb) – lit8 -	- ( <del>C</del> )					
Status Affected:	DC, N, OV,	Z, C					
Encoding:	1110	0001	1www	wBkk	k11k	kkkk	
Description:	instruction i	Vb) – lit8 – (Ö s equivalent i is not stored.	to the SUBB i	nstruction, bu	it the result o	f the	
	The 'B' bit s	select the ad selects byte o provide the li	r word opera	tion ('0' for w	ord, '1' for by		
	1	The extension rather than a denote a word The Z flag is "	word operation d operation, b	on. You may i out it is not re	use a . W exte quired.	ension to	
	i	nstructions ca	an only clear	Z.			
Words:	1						
Cycles:	1						
Example 1: CPI	B.B W4, #0	x12 ; Co	ompare W4 wi	ith 0x12 us	ing C (Byte	mode)	
W4 SF		-	After Instruction V4 7711 SR 0008	(N = 1)			
Example 2: CPB	3.B ₩4, #0>	(12 ; Cor	npare W4 wi	th 0x12 usi	.ng C (Byte	mode)	
W4 SR		W		N = 1)			
Example 3: CPB	W12, #0	)x1F ; Cor	npare W12 w	ith 0x1F us	ing C (Word	d mode)	
W12 SR <u>Example 4:</u> CPB	0002 (Z	,	R 0003 (	Z,C=1) ith 0x1F us	ing C (Word	l mode)	
W12 SR		W1: C = 1) SF		C = 1)			

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	CPB{.B}	Wb,	Ws		
-	-			[Ws]		
				[Ws++]		
				[Ws]		
				[++Ws]		
				[Ws]		
Operands:	Wb ∈ [W0 . Ws ∈ [W0 .					
Operation:	(Wb) – (Ws	s) – ( <del>C</del> )				
Status Affected:	DC, N, OV,	Z, C				
Encoding:	1110	0001	1www	wB00	0ррр	SSSS
	Register dir The 'w' bits The 'B' bit s The 'p' bits The 's' bits	rect or indirec select the ad selects byte o select the so select the add	at addressing Idress of the N or word operat urce Address dress of the V	Ns source reg	for Ws. gister. ord, '1' for byt gister.	te).
	I	rather than a	word operatic	struction deno on. You may u out it is not req	ise a .W exte	
		The Z flag is " instructions ca	•	DC, CPB, S Z.	UBB and SUE	3BR. These
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-m	nodify-write op	perations on n	non-CPU Spec	ycle count doe cial Function F r <mark>cle Instructio</mark>	Registers. For	
read-m details,	nodify-write op s, see <b>Note 3</b> i	perations on n in <b>Section 3.2</b> [W1++] ; Co	non-CPU Spec 2.1 "Multi-Cy	cial Function F cle Instructio with W0 usi	Registers. For ons".	r more

Example 2:

	;	; Post-increment W1	
	Before	After	
I	nstruction	Instruction	
W0	ABA9	W0 ABA9	
W1	1000	W1 1001	
Data 1000	D0A9 Dat	ta 1000 D0A9	
SR	0001 (C = 1)	SR 0001 (C = 1)	
Example 3: CPB	W4, W5	; Compare W5 with W4 using $\overline{\text{C}}$ (Word mode)	
	Before	After	
Ir	struction	Instruction	
W4	4000	W4 4000	
W5	3000	W5 3000	
SR	0001 (C = 1)	SR 0001 (C = 1)	

CPB.B W0, [W1++] ; Compare [W1] with W0 using  $\overline{C}$  (Byte mode)

CPBEQ		Compare W	b with Wn,	Branch if Eq	ual (Wb = V	/n)
Implemented in	: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	CPBEQ{.B}	Wb,	Wn, Expr		
Operands:	$Wb \in [W0]$ $Wn \in [W0]$					
Operation:	(Wb) – (Wr If (Wb) = (V	ו) Vn), [(PC+2) -	+ 2 * Expr] –	→PC and NOF	P →Instructio	n Register
Status Affected:	None					
Encoding:	1110	0111	1www	wBnn	nnnn	SSSS
Description:	subtraction next instruc discarded, specified b	ne contents o (Wb) – (Wn) ction (fetched the PC is rec. y Expr, and o n), the next in:	, but do not s during the c alculated bas n the next cy	store the resu urrent instruc sed on the 6- rcle, a NOP is	It. If (Wb) = ( tion execution bit signed off executed inst	(Wn), the on) is fset stead. If
	The 'B' bit : The 's' bits	select the ac selects byte o select the ad select the off	r word opera dress of the	ation ('0' for w Wn source re	vord, '1' for b egister.	yte).
		The extension rather than a denote a wor	word opera	tion. You ma	y use a .W	
Words:	1					
Cycles:	1 (5 if bran	ch taken)				
	002000 HERE:CP 002002 ADD W2, 002004 002006 002008 BYPASS: 00200A	W3, W4; Pe  				e),
,	Before Instruction           PC         00 2000           W0         1000           W1         1000           SR         00000	)	PC W0 W1 SR	After Instruction 00 2008 1000 1000 0002 (	(z = 1)	

CPBGI	Signed Co	mpare Wb wit	h Wn, Bran	ch if Greate	r Than (Wb	> Wn)
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	CPBGT{.B}	Wb,	Wn, Expr		
Operands:	$Wb \in [W0]$ $Wn \in [W0]$					
Operation:	(Wb) – (Wr If (Wb) = (V	ı) Vn), [(PC+2) +	2 * Expr] →	PC and NOP	→Instructio	n Register
Status Affected:	None					
Encoding:	1110	0110	0www	wBnn	nnnn	SSSS
	next instruct discarded, specified by (Wb) ≠ (Wr taken).	(Wb) – (Wn), I ction (fetched d the PC is recal y Expr, and on a), the next inst select the add	luring the cu culated base the next cyc ruction is ex	rrent instructi ed on the 6-b le, a NOP is e ecuted as no	ion execution it signed offer executed insormal (branc	n) is set tead. If
	The 'B' bit s The 's' bits	selects byte or select the add select the offs	word operat ress of the V	ion ('0' for wo Vn source reg	ord, '1' for by gister.	yte).
		The extension rather than a v denote a word	word operati	on. You may	use a .W e	
Words:	1					
Cycles:	1 (5 if brand	ch taken)				
<u>Example 1:</u>	002000 HERE: 002002 002004 002006 002008 BYPASS 00200A	· · · · · ·	, W1, BYPA , W3, W4		> W1 (Byte m branch t	
	Before Instruction PC 00 200 W0 30F W1 26F SR 000	00 FF E	PC W0 W1 SR	After Instruction 00 2008 00FF 26FE 0000	(N, C = 0)	

CFDLI	Signed Co	mpare wb w	ith wh, Brar	ich if Less I	nan (wb < v	vnj
Implemented	n: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
			Х			Х
Syntax:	{label:}	CPBLT{.B}	Wb,	Wn, Expr		
Operands:	$Wb \in [W0]$ $Wn \in [W0]$					
Operation:	(Wb) – (Wr If (Wb) = (V	ı) Vn), [(PC+2) -	+ 2 * Expr] →	PC and NOP	→Instructior	n Register
Status Affecte	d: None					
Encoding:	1110	0110	1www	wBnn	nnnn	SSSS
	discarded, by Expr, an the next ins	ction (fetched the PC is reca d on the next struction is ex select the ad	lculated base cycle, a NOP ecuted as no	ed on the 6-bi is executed rmal (branch	t signed offse instead. If (W is not taken)	ét specifieo /b) ≠ (Wn)
	The 'B' bit s The 's' bits	selects byte o select the ad select the off	r word opera dress of the \	tion ('0' for w Nn source re	ord, '1' for by gister.	rte).
		The extensio rather than a denote a wor	word operat	ion. You may	yuse a .W e	
Words:	1					
Cycles:	1 (5 if bran	ch taken)				
Example 1:	002000 HERE: 002002 002004 002006 002008 BYPASS: 00200A	ADD W2, W3  		SS; If W8 < orm branch		node),
	Before Instruction PC 00 2000 W8 00FF W9 26FE SR 0000		PC W8 W9 SR	After nstruction 00 2008 00FF 26FE 0008 (N	√ = 1)	

#### **CPBLT** Signed Compare Wb with Wn, Branch if Less Than (Wb < Wn)

CPBNE		Compare Wi	o with Wn, B	ranch if Not E	Equal (Wb ≠ \	Vn)
Implemented in	n: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	CPBNE{.B}	Wb,	Wn, Expr		
Operands:	$Wb \in [W0]$ $Wn \in [W0]$					
Operation:	(Wb) – (Wr If (Wb) = (V	ו) Vn), [(PC+2) +	- 2 * Expr] →	PC and NOP	→Instruction	Register
Status Affected	I: None					
Encoding:	1110	0111	0www	wBnn	nnnn	SSSS
	and on the instruction The 'w' bits	ecalculated ba next cycle, a f is executed as select the add	NOP is execut normal (brai dress of the \	ted instead. If nch is not take Nb source reg	(Wb) ≠ (Wn) en). gister.	, the next
	The 's' bits	selects byte or select the ado select the offs	lress of the V	Vn source reg	ister.	e).
	Note:	The extension rather than a denote a word	word operat	tion. You may	use a .W e	
Words:	1					
Cycles:	1 (5 if bran	ch taken)				
<u>Example 1:</u>	002000 HERE: 002002 002004 002006 002008 BYPASS 00200A	ADD W2, W  		PASS ; If W2 form branch		ce mode),
	Before Instructio PC 00 200 W2 000 W3 26F SR 000	00 =F =E	PC   W2   W3   SR	After Instruction 00 200A 00FF 26FE 0001 (	C = 1)	

CPSEQ	7:0045		Wb with Wn, s			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х		Х	Х	<u> </u>
Syntax:	{label:}	CPSEQ{.B}	Wb,	Wn		
Operands:	Wb ∈ [W0 . Wn ∈ [W0 .					
Operation:	(Wb) – (Wn Skip if (Wb)	n)				
Status Affected:	None					
Encoding:	1110	0111	1www	wB00	0000	SSSS
	next instruc discarded a (Wb) ≠ (Wn The 'w' bits	ction (fetched and on the ne n), the next in s select the ad	), but do not s d during the cu ext cycle, a No nstruction is e uddress of the	Current instruc OP is execute executed as n Wb source re	ction executio ed instead. If normal. register.	on) is f
	The 'B' bit s The 's' bits	selects byte c s select the ad	or word opera ddress of the '	ation ('0' for w Wn source re	word, '1' for b egister.	
		rather than a	on . B in the a word operation,	ation. You ma	ay use a .W	
Words:	1					
Cycles:	1 (2 or 3 if s	skip taken)				
00 00 00 00	02000 HERE:CP 02002GOTOBYPA 02004 02006 02008 BYPASS: 0200A	ASS; skip th		W1 (Byte mc	ode),	
	Before			After		
_	Instruction			Instruction		
	PC 00 2000		PC	00 2002		
	V0 1001 V1 1000		W0 W1	1001		
	SR 0000		SR	0000		
01	018000 HERE: 018002 018006 018008		↓, W8; If W4 FIR; skip th			
	Before Instruction PC 01 8000		lr PC	After nstruction 01 8006		

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CPSEQ	2	Compare W	b with Wn,	Skip if Equa	l (Wb = Wn)	
Implemented in	n: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	CPSEQ{.B}	Wb,	Wn		
Operands:	$Wb \in [W0]$ $Wn \in [W0]$					
Operation:	(Wb) – (W Skip if (W	,				
Status Affected	I: None					
Encoding:	1110	0111	1www	wB00	0001	SSSS
	next instru discarded (Wb) ≠ (W The 'w' bit The 'B' bit	n (Wb) – (Wn) action (fetched and on the ne 'n), the next in as select the ac selects byte o s select the ad	during the ca xt cycle, a No struction is e Idress of the or word opera	urrent instruc DP is execute xecuted as n Wb source n ation ('0' for w	tion execution d instead. If ormal. egister. vord, '1' for b	on) is
	Note:	The extension rather than a denote a wor	n .B in the word opera	instruction d tion. You ma	enotes a by y use a .W e	
Words:	1		,			
Cycles:	1 (2 or 3 if	skip taken)				
<u>Example 1:</u>	002000 HERE:C 002002GOTOBYP 002004 002006 002008 BYPASS 00200A	ASS; skip th  		W1 (Byte mc	ode),	
	Before           Instruction           PC         00 200           W0         100           W1         100           SR         000	0 1 0	PC W0 W1 SR	After Instruction 00 2002 1001 1000 0000		

Example 2:	0180 0180 0180 0180	006	CPSEQ CALL 		W4 = W8 (Wo the subrout	
		Before Instruction			After Instruction	
	PC	01 8000	]	PC	01 8006	
	W4	3344		W4	3344	
	W8	3344		W8	3344	
	SR	0002	(Z = 1)	SR	0002	(Z = 1)

CPSGT	Signed C	ompare Wb wi	th Wn, Skip i	if Greater Tl	han (Wb > V	Vn)
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х		Х	Х	
Syntax:	{label:}	CPSGT{.B}	Wb,	Wn		
Operands:	Wb∈ [W0 Wn∈ [W0					
Operation:	(Wb) – (W Skip if (W	,				
Status Affected:	None					
Encoding:	1110	0110	0www	wB00	0000	SSSS
	next instru discarded the next ir	n (Wb) – (Wn), action (fetched a and on the nex astruction is exe as select the ada	during the cur t cycle, a NOF cuted as nor	rent instructi P is executec mal.	ion executio I instead. Ot	n) is
	The 'B' bit	selects byte or select the add	word operati	on ('0' for wo	ord, '1' for by	yte).
	Note:	The extension rather than a denote a word	word operation	on. You may	use a .W e	
Words:	1					
Cycles:	1 (2 or 3 i	skip taken)				
Example 1:	002000 HERE 002002 002006 002008 00200A BYPAS 00200C	GOTO 	WO, W1; If BYPASS; ski	• •	yte mode),	
	Before	<u>!</u>		After		
	Instructi			Instruction		
	PC 00 20		PC	00 2006		
			W0	00FF		
	W1 26	FF FE 009 (N, C = 1)	W0 W1 SR	00FF 26FE	(N, C = 1)	
Example 2:	W1 26	FE 009 (N, C = 1) CPSGT W	W1	00FF 26FE 0009 4 > W5 (Wo	rd mode),	
Example 2:	W1 26 SR 00 018000 HERE: 018002 018006 018008 Before	FE           009         (N, C = 1)           CPSGT         W           CALL         _	W1 SR 4, W5; If W FIR; skip t	00FF 26FE 0009 4 > W5 (Wo he subrout. After	rd mode),	
<u>Example 2:</u>	W1 26 SR 00 018000 HERE: 018002 018006 018008 Before Instructio	FE         009         (N, C = 1)           CPSGT         W           CALL         _               n	W1 SR 4, W5; If W FIR; skip t 	00FF 26FE 0009 4 > W5 (Wo he subrout. After astruction	rd mode),	
<u>Example 2:</u>	W1 26 SR 00 018000 HERE: 018002 018006 018008 Before Instructio PC 0180	FE 109 (N, C = 1) CPSGT W CALL _  n 100	W1 SR 4, W5; If W FIR; skip t PC	00FF 26FE 0009 4 > W5 (Wo he subrout. After istruction 01 8002	rd mode),	
<u>Example 2:</u>	W1 26 SR 00 018000 HERE: 018002 018006 018008 Before Instructio	FE 109 (N, C = 1) CPSGT W CALL _  n 00 00	W1 SR 4, W5; If W FIR; skip t 	00FF 26FE 0009 4 > W5 (Wo he subrout. After astruction	rd mode),	

#### **CPSGT** Signed Compare Wb with Wn, Skip if Greater Than (Wb > Wn)

Implemented in:	: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
			Х			Х
Syntax:	{label:}	CPSGT{.B}	Wb,	Wn		
Operands:	Wb∈ [W0 Wn∈ [W0					
Operation:	(Wb) – (W Skip if (Wt	,				
Status Affected:	None					
Encoding:	1110	0110	0www	wB00	0001	SSSS
	next instru discarded the next in The 'w' bit The 'B' bit	n (Wb) – (Wn), ction (fetched of and on the new struction is exe s select the ad selects byte of	during the cu kt cycle, a NO ecuted as nor dress of the <sup>N</sup> word operat	rrent instruct P is executed rmal. Wb source re tion ('0' for we	ion executio d instead. Of gister. ord, '1' for b	n) is therwise,
	Note:	s select the add The extension rather than a denote a word	n .B in the i word operati	nstruction de ion. You may	notes a byte use a .W e	
Words:	1					
Cycles:	1 (2 or 3 if	skip taken)				
Example 1:	002000 HERE: 002002 002006 002008 00200A BYPAS 00200C	GOTO  		W0 > W1 (B ip the GOTO	yte mode),	
	Before			After		
	Instructio			Instruction		
	PC 00 20	00	PC	00 2006		
	W0 00	FF	W0	00FF		
	W1 26		W1	26FE		
	SR 00	09 (N, C = 1)	SR	0009	(N, C = 1)	
Example 2:	018000 HERE: 018002 018006 018008			W4 > W5 (Wo the subrout		
	Before			After		
	Instruction			nstruction		
	PC 01 800	0	PC	01 8002		
			14/4			
	W4 260 W5 260	0	W4 W5	2600 2600		

#### **CPSGT**

Signed Compare Wb with Wn, Skip if Greater Than (Wb > Wn)

CPSLI	Signed Co	ompare Wb w	ith Wn, Skip	o if Less Tha	n (Wb < Wn)	
Implemented i	n: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х		Х	Х	
Syntax:	{label:}	CPSLT{.B}	Wb,	Wn		
Operands:	Wb∈ [W0 Wn∈ [W0					
Operation:	(Wb) – (Wi Skip if (Wb					
Status Affecte	d: None					
Encoding:	1110	0110	1www	wB00	0000	SSSS
	next instru discarded next instru	n (Wb) – (Wn) ction (fetched and on the ne ction is execu s select the ac	during the co xt cycle, a NO ted as norma	urrent instruct P is executed II.	ion execution instead. Oth	n) is
	The 'B' bit	selects byte c select the ad	or word opera	tion ('0' for w	ord, '1' for by	∕te).
	Note:	rather than a	a word opera	instruction de tion. You may but it is not re	yusea.We	
Words:	1					
Cycles:	1 (2 or 3 if	skip taken)				
Example 1:	002000 HERE: 002002 002006 002008 00200A BYPASS 00200C	CPSLT.B GOTO   		W8 < W9 (B ip the GOTO		
	Before			After		
	Instruction			nstruction		
	PC 00 200		PC	00 2002		
	W8 00FI		W8	00FF		
	W9         26FE           SR         0008	= 8 (N = 1)	W9 SR	26FE 0008 (N	N = 1)	
Example 2:	018000 HERE: 018002 018006 018008			W3 < W6 (Wo the subrout:		
	Before Instructio PC 01 800 W3 260	00	PC W3	After Instruction 01 8006 2600		
	W6 300		W6	3000		
	SR 000		SR	0000		

## **CPSLT** Signed Compare Wb with Wn, Skip if Less Than (Wb < Wn)

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	CPSLT{.B}	Wb,	Wn		
Operands:	Wb ∈ [W0 Wn ∈ [W0					
Operation:	(Wb) – (Wn Skip if (Wb)	,				
Status Affected:	None	, 				
Encoding:	1110	0110	1www	wB00	0001	SSSS
Description:	subtraction next instruct discarded a next instruct	he contents of (Wb) – (Wn), ction (fetched and on the ney ction is execut	), but do not s I during the cu ext cycle, a NO uted as norma	store the resul urrent instruct )P is executed al.	It. If (Wb) < (\ tion execution d instead. Oth	Wn), the n) is
	The 'B' bit s	s select the ad selects byte o s select the ad	or word opera	ation ('0' for w	vord, '1' for by	∕te).
		rather than a	a word operat	instruction de ation. You may but it is not re	iy use a .W e	
Words:	1					
Cycles:	1 (2 or 3 if s	skip taken)				
00 00 00 00	02000 HERE: 02002 02006 02008 02008 BYPASS: 0200C	GOTO  		<sup>:</sup> W8 < W9 (B ip the GOTO		
	Before			After		
-	Instruction			Instruction		
	PC 00 2000 V8 00FF		PC W8	00 2002 00FF		
	V8 00FF V9 26FE		W8 W9	26FE		
		8 (N = 1)	SR	0008 (N	<b>√</b> = 1)	
(	018000 HERE: 018002 018006 018008			W3 < W6 (Wo the subrout		
	Before Instruction PC 01 800		PC	After Instruction 01 8006		
	W3 260	00	W3	2600	I	
	W6 300	<b>—</b> 1	W6	3000	1	

CPSLT	Signed Compare Wb with Wn, Skip if Less Than (Wb < V
	eighea eempare the than thi, eiap in 2000 man (the vi

Implemented in	: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
implemented in	X	X	11024	X	X	
Syntax:	{label:}	CPSNE{.B}	Wb,	Wn		
Operands:	$Wb \in W0$ $Wn \in W0$	-				
Operation:	(Wb) – (Wr Skip if (Wb					
Status Affected	None					
Encoding:	1110	0111	0www	wB00	0000	SSSS
	instruction and on the instruction	(Wb) – (Wn), (fetched during next cycle, a f is executed as select the add	g the current NOP is execut s normal.	instruction ex ted instead. O	ecution) is di therwise, the	scarded
	The 'B' bit s	selects byte or select the add	word operat	ion ('0' for wo	rd, '1' for byt	e).
		The extension rather than a denote a word	word operat	ion. You may	use a .We	•
Words:	1		-		-	
Cycles:	1 (2 or 3 if :	skip taken)				
	002000 HERE: 002002 002006 002008 00200A BYPASS 00200C	GOTO  		<sup>=</sup> W2 != W3 ( kip the GOTO		,
	Before			After		
	Instructio			Instruction		
	PC 00 200 W2 00F		PC W2	00 2006 00FF		
	W3 26F		W2 W3	26FE		
		01 (C = 1)	SR	0001 (	C = 1)	
	018000 HERE: 018002 018006 018008			WO != W8 (W the subrout		
	Before Instructio PC 01 800 W0 300 W8 300	00 00	PC W0 W8	After Instruction 01 8002 3000 3000		

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
·			Х			Х
Syntax:	{label:}	CPSNE{.B}	Wb,	Wn		
Operands:	Wb ∈ [W0 . Wn ∈ [W0 .	-				
Operation:	(Wb) – (Wn Skip if (Wb)	י- ו)				
Status Affected:	None					
Encoding:	1110	0111	0www	wB00	0001	SSSS
	instruction ( and on the instruction i	(Wb) – (Wn), (fetched during next cycle, a N is executed as	g the current NOP is execut s normal.	instruction ex ted instead. O	xecution) is dia Dtherwise, the	iscarded
	The 'B' bit s	s select the add selects byte or select the add	r word operati	tion ('0' for wo	ord, '1' for byte	e).
	I	The extension rather than a denote a word	word operat	tion. You may	yuse a.We	
Words:	1		104-		Junes	
Cycles:	- 1 (2 or 3 if s	skip taken)				
000 000 000 000	02000 HERE: 02002 02006 02008 0200A BYPASS 0200C	GOTO I  		f W2 != W3 ( kip the GOTO		
	Before			After		
	Instruction			Instruction		
	PC 00 200		PC	00 2006		
	V2 00F V3 26F		W2 W3	00FF 26FE		
		-E 01 (C = 1)	SR	0001 (0	(C = 1)	
01	118000 HERE: 118002 118006 118008			WO != W8 (W the subrout		
	Before Instruction PC 01 800 W0 300	on	PC W0	After Instruction 01 8002 3000		

# 

DAW.B		Decimal Ad	just Wn			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	DAW.B	Wn			
Operands:	Wn∈ [W0	W15]				
Operation:	(Wn<3:0 Else	> > 9) or (DC  >) + 6 →Wn<  >) →Wn<3:0;	3:0>			
	(Wn<7:4 Else	> > 9) or (C = >) + 6 ->Wn< >) ->Wn<7:42	7:4>			
Status Affected:	С					
Encoding:	1111	1101	0100	0000	0000	SSSS
	Carry flag i addressing The 's' bits Note 1: 2:	It. The Most s s used to indi must be use select the so This instructio packed BCD This instructio extension mu	cate any dec d for Wn. urce/destinat on is used to bytes have b on operates i	timal rollover. tion register. correct the d leen added. n Byte mode	Register direction at a format af only and the	ect ter two
Words:	1					
Cycles:	1					
Example 1:	DAW.B W0	; Decir	nal adjust	WO		
	Before Instruction W0 771A SR 0002 (	١	After Instruction W0 7720 SR 0002	) (DC = 1)		
Example 2:	DAW.B W3	; Decir	nal adjust	W3		
	Before Instruction W3 77AA SR 0000		After Instruction /3 7710 R 0001 (1	C = 1)		
# **Section 5. Instruction Descriptions**

DEC		Decrement	f			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	DEC{.B}	f	{,WREG}		
Operands:	f∈ [0 81	91]				
Operation:	(f) – 1 →de	stination desig	gnated by D			
Status Affected:	DC, N, OV,	Z, C				
Encoding:	1110	1101	0BDf	ffff	ffff	ffff
Description:	destination destination WREG is n	e from the co register. T register. If W ot specified, t selects byte o	he optional REG is spec he result is s	WREG op ified, the result tored in the fi	erand deter ult is stored i le register.	mines the n WREG. If
	The 'D' bit s	selects the de select the add	stination ('0'	for WREG, '1		
	1	The extensior rather than a denote a word The WREG is	word operatio d operation, b	on. You may u out it is not re	use a .W exte quired.	
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-mo	dify-write op	C24E devices, erations on no Section 3.2.	on-CPU Spec	ial Function F	Registers. For	
Example 1: D	EC.B 0x20	0	; Decremen	it (0x200) (	(Byte mode)	
Data 20 S	Before Instruction 00 80FF R 0000	Data 2	-	n ] (N, C = 1)		
Example 2: DE	C RAM40	0, WREG ;	; Decrement ; (Word mod	RAM400 and e)	store to N	WREG
WREG RAM40 SI	0 0823	WRE RAM40 S				

DEC		Decrement	Ws			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	DEC{.B}	Ws,	Wd		
- <b>,</b>	(	- ( )	[Ws],	[Wd]		
			[Ws++],	[Wd++]		
			[Ws],	[Wd]		
			[++Ws],	[++Wd]		
			[Ws],	[Wd]		
Operands:	Ws ∈ [W0 . Wd ∈ [W0 .					
Operation:	$(Ws) - 1 \rightarrow$	Wd				
Status Affected:	DC, N, OV,	Z, C				1
Encoding:	1110	1001	0Bqq	qddd source regist	dppp	SSSS
	The 'B' bit s The 'q' bits The 'd' bits The 'p' bits	may be used selects byte o select the de select the de select the sou select the sou	r word opera stination Add stination regi urce Address	tion ('0' for wo ress mode. ster.	ord, '1' for by	te).
		rather than a	word operat	instruction de tion. You may but it is not re	/usea.We	
Words:	1		·			
Cycles:	1 <sup>(1)</sup>					
read-mo	odify-write op	erations on ne	on-CPU Spec	cle count doe: ial Function F cle Instructio	Registers. For	
Example 1: DEC	.B [W7++],			and store t ement W7, W		e mode)
W7 W8 Data 2300 Data 2400 SR	Before Instruction 2301 2400 5607 ABCD 0000	W W Data 230 Data 240 Sf	8 2401 0 5607 0 AB55			

0009 (N, C = 1)

Example 2: ; Decrement W5 and store to [W6] (Word mode) DEC W5, [W6++] ; Post-increment W6 Before After Instruction Instruction D004 D004 W5 W5 2000 2002 W6 W6 Data 2000 ABA9 Data 2000 D003

SR

SR

0000

5

DEC2		Decrement	f by 2			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	DEC2{.B}	f	{,WREG}		
Operands:	f∈ [0 81	91]				
Operation:	(f) – 2 →de	stination desi	gnated by D			
Status Affected:	DC, N, OV,	Z, C				
Encoding:	1110	1101	1BDf	ffff	ffff	ffff
Description:	destination destination WREG is n	o from the co register. T register. If W ot specified, t	he optional REG is spec he result is s	WREG op ified, the resu tored in the fi	erand deter ult is stored i le register.	mines the n WREG.
	The 'D' bit s	selects byte o selects the de select the ado	stination ('0'	for WREG, '1		
		The extension rather than a denote a wor	word operat	tion. You may	/usea.We	•
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-me details, <u>Example 1:</u> D	odify-write op see <b>Note 3</b> ir EC2.B 0x2 Before Instruction		on-CPU Spec 1 "Multi-Cyc ; Decrement After Instruction	ial Function F ile Instructio	Registers. For ns".	more
	R 0000	Data 2	SR 0009	(N, C = 1)	2 and	
<u> </u>	Before			WREG (Word		

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	х
Syntax:	{label:}	DEC2{.B}	Ws,	Wd		
			[Ws],	[Wd]		
			[Ws++],	[Wd++]		
			[Ws],	[Wd]		
			[++Ws],	[++Wd]		
			[Ws],	[Wd]		
Operands:	Ws ∈ [W0 Wd ∈ [W0	-				
Operation:	(Ws) – 2 $\rightarrow$	Wd				
Status Affected:	DC, N, OV,	Z, C				
Encoding:	1110	1001	1Bqq	qddd	dppp	SSSS
Description:	result in the		register Wd.	source regis Either registe Wd.		
	The 'q' bits The 'd' bits The 'p' bits	selects byte o select the de select the de select the so select the so	stination Add stination regi urce Address	ister. s mode.	ord, '1' for by	∕te).
		rather than a	word opera	instruction de tion. You may but it is not re	yusea.We	
Words:	1		• •			
Cycles:	1 <sup>(1)</sup>					
read-mo	dify-write ope	erations on no	n-CPU Spec	cle count does ial Function R I <b>e Instructio</b> n	egisters. For	

Example 1:	DEC2.B [W7], [W	/8]; DEC [W7] by 2,	store to [W8]	(Byte mode)
		; Post-decreme	nt W7, W8	

I	Before nstructior	1 I	After nstructior	ı
W7	2301	W7	2300	
W8	2400	W8	23FF	
Data 2300	0107	Data 2300	0107	
Data 2400	ABCD	Data 2400	ABFF	
SR	0000	SR	0008	(N = 1)

; DEC W5 by 2, store to [W6] (Word mode) Example 2: DEC2 W5, [W6++] ; Post-increment W6 After Before Instruction Instruction D004 W5 D004 W5 1000 1002 W6 W6 Data 1000 Data 1000 D002 ABA9 0009 (N, C = 1) SR 0000 SR

DISI		Disable Inte	errupts Tem	porarily		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	DISI	#lit14			
Operands:	lit14 ∈ [ 0	16383]				
Operation:	lit14 →DIS 1 →DISI Disable int	ICNT errupts for (lit	14 + 1) cycle	S		
Status Affected:	None					
Encoding:	1111	1100	00kk	kkkk	kkkk	kkkk
	Note 1: 2:	ime critical co This instruction from running. for details. This instruction device is in S	on does not p See the spe on does not p	prevent priori cific device f	ty 7 interrupt amily referer	ice manual
Words:	1					
Cycles:	1					
002	000 HERE: 002 004	DISI #10 		le interrup 00 cycles p		
PC DISICNT INTCON2		) )	PC DISICNT INTCON2	After nstruction 00 2002 0100 4000 (	(DISI = 1)	
SR	0000	)	SR	0000	-	

DIV.S	Signed Integer Divide							
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	DIV.S{W} DIV.SD	Wm, Wn Wm, Wn					
Operands:		0, W2, W4	word operati W14] for dou		n			
Operation:	Wm →V <u>If (Wm&lt;:</u> 0xFFF <u>Else:</u> 0x0 - W1:W0 /	<u>15&gt; = 1):</u> F →W1	<u>ault):</u>					
Status Affaatad	Wm + 1: W1:W0 / Remaind	operation (D Wm →W1:W ′ Wn →W0 der →W1						
Status Affected: Encoding:	N, OV, Z, C	, 1000	0ttt	tvvv	v₩00	SSSS		
Description:	16-bit by 16 the divisor copied to V the double quotient of is stored in This instruct (with an ite remainder. otherwise. overflow ar '0' and clea algorithm a The 't' bits operation.	5-bit divide) o is stored in W VO and sign-e operation, W the divide op W1. ction must be ration count of The N flag w The OV flag w The OV flag w and cleared oth ared otherwise nd its final va select the mo These bits are select the lea	divide, where r Wm + 1:Wn /n. In the defa extended thro m + 1:Wm is eration is stor executed 18 of 17) to gene ill be set if the will be set if the will be set if the exercise. The e. The C flag due should no ost significant e clear for the ast significant	n (for a 32-bir ault word ope ugh W1 to pe first copied to red in W0, ar times using to rate the corre e remainder i ne divide ope Z flag will be is used to im ot be used. word of the c word of the c	t by 16-bit divertion, Wm is erform the op o W1:W0. Th and the 16-bit is the REPEAT is ect quotient as s negative ar eration resulted set if the rem aplement the dividend for the tion. dividend.	vide) and s first eration. In e 16-bit remainder nstruction and cleared ed in an nainder is divide		

	Note 1: 2:	The extension . D in the instruction denotes a double word (32-bit) dividend rather than a word dividend. You may use a .W extension to denote a word operation, but it is not required. Unexpected results will occur if the quotient can not be represented in 16 bits. When this occurs for the double operation (DIV.SD), the OV Status bit will be set and the quotient and remainder should not be used. For the word operation (DIV.S), only one type of overflow may occur (0x8000/0xFFFF = + 32768 or 0x00008000), which allows the OV Status bit to interpret the result.
	3:	Dividing by zero will initiate an arithmetic error trap during the first cycle of execution.
	4:	This instruction is interruptible on each instruction cycle boundary.
Words:	1	
Cycles:	18 (plus 1	for REPEAT execution)
Example 1:	REPEAT #17 DIV.S W3, W	; Execute DIV.S 18 times /4  ; Divide W3 by W4 ; Store quotient to W0, remainder to W1
	Before	After
	Instruction	
	W0 5555	W0 013B
	W1 1234 W3 3000	W1 0003 W3 3000
	W4 0027	W4 0027
	SR 0000	SR 0000
Example 2:	REPEAT #17 DIV.SD W0, N	; Execute DIV.SD 18 times W12 ; Divide W1:W0 by W12 ; Store quotient to W0, remainder to W1
	Before	After
	Instruction	Instruction
	W0 2500	W0 FA6B
	W1 FF42 W12 2200	W1 EF00 W12 2200

0008 (N = 1)

SR

SR

0000

DIV.U		Unsigned I	nteger Divid	e				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	DIV.U{W} DIV.UD	Wm, Wn Wm, Wn					
Operands:		'0 W15] for '0, W2, W4 2 W15]			n			
Operation:	Wm →W 0x0 →W W1:W0/		<u>ault):</u>					
	Wm + 1: W1:W0/	<u>operation (D</u> Wm →W1:W Wns →W0 der →W1						
Status Affected:	N, OV, Z, C	r			1	1		
Encoding: Description:	1101	1000 nsigned integ	1ttt	tvvv	VW00	SSSS		
	Wm + 1:Wn operation is This instruct (with an ite remainder. divide oper will be set i to impleme The 't' bits operation. The 'v' bits The 'W' bits The 's' bits	a 16-bit by 16-bit divide), or Wm + 1:Wm (for a 32-bit by 16-bit divide) an the divisor is stored in Wn. In the word operation, Wm is first copied to W and W1 is cleared to perform the divide. In the double operation, Wm + 1:Wm is first copied to W1:W0. The 16-bit quotient of the divide operation is stored in W0, and the 16-bit remainder is stored in W1. This instruction must be executed 18 times using the REPEAT instructior (with an iteration count of 17) to generate the correct quotient and remainder. The N flag will always be cleared. The OV flag will be set if th divide operation resulted in an overflow and cleared otherwise. The Z fla will be set if the remainder is '0' and cleared otherwise. The C flag is use to implement the divide algorithm and its final value should not be used. The 't' bits select the most significant word of the dividend for the double operation. These bits are clear for the word operation. The 'v' bits select the least significant word of the dividend. The 'W' bit selects the dividend size ('0' for 16-bit, '1' for 32-bit).						
	<ol> <li>Note 1: The extension . D in the instruction denotes a double word (32-bit) dividend rather than a word dividend. You may use a .W extension to denote a word operation, but it is not required.</li> <li>2: Unexpected results will occur if the quotient can not be represented in 16 bits. This may only occur for the double operation (DIV.UD). When an overflow occurs, the OV Status bit will be set and the quotient and remainder should not be used.</li> <li>3: Dividing by zero will initiate an arithmetic error trap during the first cycle of execution.</li> <li>4: This instruction is interruptible on each instruction cycle</li> </ol>							
Words:	1	boundary.						
Cycles:		for REPEAT e	xecution)					
- ,	(8.00 1 1							

Example 1:	REPEAT #17 DIV.U W2, W4	; Execute DIV.U 18 times ; Divide W2 by W4 ; Store quotient to W0, remainder to W1
	Before           Instruction           W0         5555           W1         1234           W2         8000           W4         0200           SR         0000	After Instruction W0 0040 W1 0000 W2 8000 W4 0200 SR 0002 (Z = 1)
Example 2:		; Execute DIV.UD 18 times ; Divide W11:W10 by W12 ; Store quotient to W0, remainder to W1
	Before	After
	Instruction	Instruction
	W0 5555	W0 01F2
	W1 1234	W1 0100
	W10 2500	W10 2500
	W11 0042	W11 0042
	W12 2200	W12 2200
	SR 0000	SR 0000

5

DIVF		Fractional [	Divide						
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
				Х	Х	Х			
Syntax:	{label:}	DIVF	Wm, Wn						
Operands:	Wm∈[W Wn∈[W								
Operation:	0x0 →W0 Wm →W1 W1:W0/Wr Remainde	ו →W0							
Status Affected:	N, OV, Z, 0								
Encoding:	1101	1001	0ttt	t000	0000	SSSS			
	W0 is first cleared and Wm is copied to W1. The 16-bit quotient of divide operation is stored in W0, and the 16-bit remainder is stored The sign of the remainder will be the same as the sign of the divide This instruction must be executed 18 times using the REPEAT instr (with an iteration count of 17) to generate the correct quotient and remainder. The N flag will be set if the remainder is negative and cl otherwise. The OV flag will be set if the divide operation resulted in overflow and cleared otherwise. The Z flag will be set if the remainder is the divide algorithm and its final value should not be used.					ividend. instruction and nd cleared ed in an nainder is			
	The 't' bits select the dividend register. The 's' bits select the divisor register.								
	<ol> <li>For the fractional divide to be effective, Wm must be less than Wn. If Wm is greater than or equal to Wn, unexpected results will occur because the fractional result will be greater than or equal to 1.0. When this occurs, the OV Status bit will be set and the quotient and remainder should not be used.</li> <li>Dividing by zero will initiate an arithmetic error trap during the first cycle of execution.</li> <li>This instruction is interruptible on each instruction cycle</li> </ol>								
Words:	1	boundary.							
Cycles:	18 (plus 1	for REPEAT e	xecution)						

# **Section 5. Instruction Descriptions**

Example 1:	REPEAT #17 DIVF W8, W9	; Execute DIVF 18 times ; Divide W8 by W9 ; Store quotient to W0, remainder to W1
	Before           Instruction           W0         8000           W1         1234           W8         1000           W9         4000           SR         0000	After Instruction W0 2000 W1 0000 W8 1000 W9 4000 SR 0002 (Z = 1)
Example 2:	REPEAT #17 DIVF W8, W9	; Execute DIVF 18 times ; Divide W8 by W9 ; Store quotient to W0, remainder to W1
	Before           Instruction           W0         8000           W1         1234           W8         1000           W9         8000           SR         0000	After Instruction W0 F000 W1 0000 W8 1000 W9 8000 SR 0002 (Z = 1)
Example 3:	REPEAT #17 DIVF W0, W1	; Execute DIVF 18 times ; Divide W0 by W1 ; Store quotient to W0, remainder to W1
	Before           Instruction           W0         8002           W1         8001           SR         0000	After Instruction W0 7FFE W1 8002 SR 0008 (N = 1)

-

DO		Initialize Hardware Loop Literal						
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
				Х	Х			
Syntax:	{label:}	DO	#lit14,	Expr				
Operands:	Expr may b	lit14 $\in$ [0 16383] Expr may be an absolute address, label or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].						
Operation:	$(lit14) \rightarrow DC$ $(PC) + 4 \rightarrow$ $(PC) \rightarrow DOS$ (PC) + (2 *)	PUSH DO shadows (DCOUNT, DOEND, DOSTART) (lit14) $\rightarrow$ DCOUNT (PC) + 4 $\rightarrow$ PC (PC) $\rightarrow$ DOSTART (PC) + (2 * Slit16) $\rightarrow$ DOEND Increment DL<2:0> (CORCON<10:8>)						
Status Affected:	DA							
Encoding:	0000	1000	00kk	kkkk	kkkk	kkkk		
	0000	0000	nnnn	nnnn	nnnn	nnnn		

Description:	Initiate a no overhead hardware D0 loop, which is executed (lit14 + 1) times. The D0 loop begins at the address following the D0 instruction, and ends at the address 2 * Slit16 instruction words away. The 14-bit count value (lit14) supports a maximum loop count value of 16384, and the 16-bit offset value (Slit16) supports offsets of 32K instruction words in both directions. When this instruction executes, DCOUNT, DOSTART and DOEND are first PUSHed into their respective shadow registers, and then updated with the new D0 loop parameters specified by the instruction. The D0 level count, DL<2:0> (CORCON<8:10>), is then incremented. After the D0 loop completes execution, the PUSHed DCOUNT, DOSTART and DOEND registers are restored, and DL<2:0> is decremented. The 'k' bits specify the loop count.
	The 'n' bits are a signed literal that specifies the number of instructions that are offset from the PC to the last instruction executed in the loop.
	<ul> <li>Special Features, Restrictions: The following features and restrictions apply to the D0 instruction.</li> <li>1. Using a loop count of '0' will result in the loop being executed one time.</li> <li>2. Using a loop size of -2, -1 or 0 is invalid. Unexpected results may</li> </ul>
	<ul> <li>occur if these offsets are used.</li> <li>3. The very last two instructions of the D0 loop cannot be: <ul> <li>an instruction which changes program control flow</li> <li>a D0 or REPEAT instruction</li> </ul> </li> </ul>
	<ul> <li>Unexpected results may occur if any of these instructions are used.</li> <li>If a hard trap occurs in the second to last instruction or third to last instruction of a D0 loop, the loop will not function properly. The hard trap includes exceptions of priority level 13 through level 15, inclusive.</li> </ul>
	<ul> <li>Note 1: The D0 instruction is interruptible and supports 1 level of hardware nesting. Nesting up to an additional 5 levels may be provided in software by the user. See the specific device family reference manual for details.</li> <li>2: The linker will convert the specified expression into the offset to be used.</li> </ul>
Words:	2
Cycles:	2
	002000 LOOP6: D0 #5, END6; Initiate DO loop (6 reps) 002004 ADD W1, W2, W3; First instruction in loop 002006 002008 00200A END6: SUB W2, W3, W4; Last instruction in loop 00200C
DCOU DOSTAI DOEM CORCO	RTFF FFFFDOSTART00 2004NDFF FFFFDOEND00 200A

5

Instruction Descriptions

C C C C C C C C C C C C C C C C C C C	1C00 1C00 1C00 1C00 1C00 1C00 1C00	6 8 A C E	DEC W1, W2	; First	Init DO loc instruction the FIR88 s	
C			NOP; Last i		ion in loop	
	;	(Required	NOP filler	)		
	I	Before nstruction			After Instruction	
F	∘c □	01 C000		PC	01 C004	]
DCOUI	NT	0000	C	COUNT	0160	
DOSTA	RT	FF FFFF	D	OSTART	01 C004	
DOEN	ND	FF FFFF		DOEND	01 C014	
CORCO	DN 🗌	0000	С	ORCON	0100	(DL = 1)
9	SR	0008	(N = 1)	SR	0208	(DA, N = 1)

		Initialize Ha	•	•			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33	
		]	<u> </u>	<u> </u>	<u> </u>	Х	
Syntax:	{label:}	DO	#lit15,	Expr			
Operands:	Expr may l	lit15 $\in$ [0 32767] Expr may be an absolute address, label or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 +32767].					
Operation:	PUSH DO shadows (DCOUNT, DOEND, DOSTART) (lit15) $\rightarrow$ DCOUNT (PC) + 4 $\rightarrow$ PC (PC) $\rightarrow$ DOSTART (PC) + (2 * Slit16) $\rightarrow$ DOEND Increment DL<2:0> (CORCON<10:8>)						
Status Affected:	DA						
Encoding:	0000	1000	0kkk	kkkk	kkkk	kkkk	
	0000	0000	nnnn	nnnn	nnnn	nnnn	
	When this instruction executes, DCOUNT, DOSTART and DOEND are first PUSHed into their respective shadow registers, and then updated with the new D0 loop parameters specified by the instruction. The D0 level count, DL<2:0> bits (CORCON<8:10>), is then incremented. After the D0 loop completes execution, the PUSHed DCOUNT, DOSTART and DOEND registers are restored, and DL<2:0> is decremented.				ed with the el count, D0 loop		
	The 'n' bits	s specify the loo s are a signed l from the PC to	literal that spe				
	<ul> <li>Special Features, Restrictions: The following features and restrictions apply to the D0 instruction.</li> <li>Using a loop count of '0' will result in the loop being executed or</li> <li>Using a loop size of -2, -1 or 0 is invalid. Unexpected results occur if these offsets are used.</li> <li>The very last two instructions of the D0 loop cannot be: <ul> <li>an instruction which changes program control flow</li> <li>a D0 or REPEAT instruction</li> <li>Unexpected results may occur if any of these instructions are used</li> </ul> </li> </ul>				ed one tim sults may		
	4. If a ha instruc trap in	ard trap occurs ction of a D0 lo ncludes excepti	s in the secon oop, the loop ions of priority	ond to last inst o will not funct y level 13 thro	truction or thi tion properly. Tugh level 15, i	ird to last The hard inclusive.	
	Note 1:	rst instruction o The D0 instruct hardware nest provided in so reference mar The linker will	ction is interru sting. Nesting oftware by the nual for detail	uptible and su up to an addi e user. See the ils.	upports 1 leve itional 5 levels e specific dev	l of s may be vice family	

Words:	2	
Cycles:	2	
-		
Example 1:	002000 LOOP6: 002004 002006 002008 00200A END6: 00200C	D0 #5, END6; Initiate D0 loop (6 reps) ADD W1, W2, W3; First instruction in loop  SUB W2, W3, W4; Last instruction in loop
	002000	
	Before Instruction PC 00 2000	After Instruction PC 00 2004
DCC	DUNT 0000	DCOUNT 0005
DOS	TART FF FFFF	DOSTART 00 2004
DC	END FF FFFF	DOEND 00 200A
COR	CON 0000	CORCON 0100 (DL = 1)
	SR 0001	(C = 1) SR 0201 (DA, C = 1)
Example 2:	01C000 L00P12: 01C004 01C006 01C008 01C00A 01C00C 01C00E 01C012 01C014 END12: ; (Require	D0 #0x160, END12; Init D0 loop (353 reps) DEC W1, W2; First instruction in loop   CALL _FIR88; Call the FIR88 subroutine NOP NOP; Last instruction in loop d NOP filler)
	Before	After
	Instruction	Instruction
	PC 01 C000	
-	DUNT 0000	
	TART FF FFF	
	DEND FF FFFF	
COF	RCON 0000 SR 0008	
	SK 0008	3 (N = 1) SR 0208 (DA, N = 1)

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC		
·				Х	Х			
Syntax:	{label:}	DO	Wn,	Expr				
Operands:		W15] be an absolute olved by the li				+327		
Operation:	PUSH Shadows (DCOUNT, DOEND, DOSTART) (Wn<13:0>) $\rightarrow$ DCOUNT (PC) + 4 $\rightarrow$ PC (PC) $\rightarrow$ DOSTART (PC) + (2 * Slit16) $\rightarrow$ DOEND Increment DL<2:0> (CORCON<10:8>)							
Status Affected:	DA							
	0000	1000	1000	0000	0000	SSS		
Encoding:	0000	0000 o overhead ha	nnnn	nnnn	nnnn	nnr		
	PUSHed into their respective shadow registers, and then updated w new D0 loop parameters specified by the instruction. The D0 level co DL<2:0> (CORCON<8:10>), is then incremented. After the D0 loop completes execution, the PUSHed DCOUNT, DOSTART and DOEN registers are restored, and DL<2:0> is decremented.				el coun cop			
	completes registers a The 's' bits	execution, the re restored, ar specify the re	e PUSHed DC nd DL<2:0> is egister Wn tha	COUNT, DOS s decremented at contains the	TART and DC d. e loop count.	DEND		
	The 'n' bits are a signed literal that specifies the number of instructions that are offset from (PC + 4), which is the last instruction executed in the loop.							
	•	atures, Rest						
		ng features ar a loop count		11.5				
	<ol> <li>Using an offset of -2, -1 or 0 is invalid. Unexpected results r if these offsets are used.</li> </ol>				nay occ			
	<ul> <li>3. The very last two instructions of the D0 loop cannot be:</li> <li>an instruction which changes program control flow</li> <li>a D0 or REPEAT instruction</li> </ul>							
	Unexpected results may occur if these last instructions are used.							
	Note 1:	The D0 instruc Nesting up to by the user. S	ction is interru an additional	uptible and su I 5 levels may	pports 1 level be provided	l of nest in softw		
		details.						
	2:	The linker will be used.	l convert the ध	specified expr	ression into th	ne offse		
Words:	2:	The linker will	l convert the ध	specified expı	ession into tr	ie offse		

Instruction Descriptions

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0020 0020 0020 0020 0020 0020 0020 002	06 08 0A 00C	DO ADD  REPEAT SUB NOP	W1, W2, W3	<pre>; Initiate D0 loop (W0 reps) ; First instruction in loop ; Last instruction in loop ; (Required NOP filler)</pre>
PC W0 DCOUNT DOSTART DOEND CORCON SR	Before Instruction 00 2000 0012 0000 FF FFFF FF FFFF FF FFFF 00000 0000		PC W0 DCOUNT DOSTART DOEND CORCON SR	After Instruction 00 2004 0012 00 2004 00 2010 0100 (DL = 1) 0080 (DA = 1)
0020 0020 0020 0020 0020	006 008	D0 SWAP   MOV	W7, ENDA W0 W1, [W2++]	; Initiate DO loop (W7 reps) ; First instruction in loop ; Last instruction in loop
PC W7 DCOUNT DOSTART DOEND CORCON SR	Before Instruction 00 2000 E00F 0000 FF FFFF FF FFFF 00000 0000		PC W7 DCOUNT DOSTART DOEND CORCON SR	After Instruction 00 2004 E00F 200F 00 2004 00 2010 0100 (DL = 1) 0080 (DA = 1)

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC3		
						Х		
Syntax:	{label:}	DO	Wn,	Expr				
Operands:		W15] be an absolute olved by the lir				+3276		
Operation:	PUSH Shadows (DCOUNT, DOEND, DOSTART) (Wn) $\rightarrow$ DCOUNT (PC) + 4 $\rightarrow$ PC (PC) $\rightarrow$ DOSTART (PC) + (2 * Slit16) $\rightarrow$ DOEND Increment DL<2:0> (CORCON<10:8>)							
Status Affected:	DA					<u>,                                    </u>		
	0000	1000	1000	0000	0000	SSSS		
Encoding:	0000	0000 o overhead ha	nnnn	nnnn	nnnn	nnnn		
	<ul> <li>PUSHed into their respective shadow registers, and then updated with the new D0 loop parameters specified by the instruction. The D0 level count, DL&lt;2:0&gt; (CORCON&lt;8:10&gt;), is then incremented. After the D0 loop completes execution, the PUSHed DCOUNT, DOSTART and DOEND registers are restored, and DL&lt;2:0&gt; is decremented.</li> <li>The 's' bits specify the register Wn that contains the loop count. The 'n' bits are a signed literal that specifies the number of instructions the</li> </ul>							
	are offset from (PC + 4), which is the last instruction executed in the loop. Special Features, Restrictions:							
	The following	ng features an	nd restrictions					
	1. Using a time.	a loop count	of '0' will res	ult in the loo	p being exec	uted one		
		an offset of -2, e offsets are u		alid. Unexpe	cted results m	ау осси		
	3. The ve	ery last two ins	structions of the					
		nstruction whic	0 1	rogram contro	ol flow			
	a D0 or REPEAT instruction							
	<ul><li>Unexpected results may occur if these last instructions are used.</li><li>The first instruction of the D0 loop cannot be a PSV read or Table read.</li></ul>							
			-					
	4. The firs Note 1:		of the DO loop of ction is interru an additional ee the specifi	cannot be a P Iptible and su 5 levels may ic device fami	PSV read or Ta pports 1 level be provided ily reference r	able read of nestir in softwa manual f		

Instruction Descriptions

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# **16-bit MCU and DSC Programmer's Reference Manual**

DO	Ini	itialize H	lardware Loc	op Wn	
Cycles:	2				
Example 1: 0020 0020 0020 0020 0020 0020	006 008	DO ADD  			00 loop (W0 reps) cruction in loop
0020 0020 0020		REPEAT SUB NOP	#6 W2, W3, W4	; Last instr ; (Required	ruction in loop NOP filler)
PC W0	Before Instruction 00 2000 0012		PC W0	After Instruction 00 2004 0012	
DCOUNT DOSTART	0000 FF FFFF		DCOUNT DOSTART	0012	
DOEND	FF FFFF		DOEND	00 2010	
CORCON SR	0000 0000		CORCON SR	<u> </u>	DL = 1) DA = 1)
0020 0020 0021 0021 0021	906 908	D0 SWAP   M0V	W7, ENDA W0	; First inst	DO loop (W7 reps) truction in loop ruction in loop
002	Before		"", [""", ]	After Instruction	
PC	00 2000		PC	00 2004	
W7 DCOUNT	E00F		W7 DCOUNT	E00F	
DCOUNT	0000 FF FFFF		DCOUNT	200F 00 2004	
DOEND	FF FFFF		DOSTART	00 2004	
CORCON	0000		CORCON		(DL = 1)
SR	0000		SR	0080 (	(DA = 1)

Implemented	d in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	ĺ				X	X	X
							<u> </u>
Syntax:	{label:}	ED	Wm * Wm,	Acc,	[Wx],	[Wy],	Wxd
						[Wy] + = ky,	
						[Wy] – = ky,	
					[W9 + W12],	[W11 + W12],	
Operands:		Wx ∈ [W8,	∈ [W4 * W4, W9]; kx ∈ [-6 ), W11]; ky ∈	6, -4, -2, 2, 4		* W7]	
Operation:		-	n) →Acc(A o /]) →Wxd →Wx	r B)			
Status Affect	ted:	OA, OB, OA	AB, SA, SB,	SAB			
Encoding:	I	1111	00mm	A1xx	00ii	iijj	jj11
		sign-extend	led to 40 bits Wx] – [Wy] ar	s and stored re stored in \	in the specifi Wxd, which n	f Wm * Wm a ied accumulat nay be the sa h operations y	tor. The .me as Wm.
		support indi		jister offset a	addressing as	s described in	
		support indi Section 4.1 The 'm' bits The 'A' bit s The 'A' bits The 'x' bits The 'i' bits s	irect and reg 14.1 "MAC F s select the o selects the ad	pister offset a Prefetches". operand regis ccumulator for refetch differo x prefetch op	addressing as ster Wm for the or the result. ence Wxd de peration.	s described in he square.	
Words:		support indi Section 4.1 The 'm' bits The 'A' bit s The 'A' bits The 'x' bits The 'i' bits s	irect and reg 14.1 "MAC F s select the o selects the ac select the pr select the Wa	pister offset a Prefetches". operand regis ccumulator for refetch differo x prefetch op	addressing as ster Wm for the or the result. ence Wxd de peration.	s described in he square.	
Cycles:		support indi Section 4.1 The 'm' bits The 'A' bit s The 'i' bits s The 'j' bits s 1 1	irect and reg 14.1 "MAC F s select the o selects the ad select the pr select the Wy select the Wy	gister offset a Prefetches". Operand regis ccumulator for refetch differo x prefetch op y prefetch op	addressing as ster Wm for the or the result. ence Wxd de peration. peration.	s described in he square. estination.	
	ED W	support indi Section 4.1 The 'm' bits The 'A' bit s The 'i' bits s The 'j' bits s 1	irect and reg 14.1 "MAC F s select the o selects the ad select the pr select the Wy select the Wy	gister offset a Prefetches". Operand regis ccumulator for refetch differo x prefetch op y prefetch op	addressing as ster Wm for the or the result. ence Wxd de peration. peration. ; Square ; [w8]-[ ; Post-i	s described in he square.	1 A 3
Cycles:	ED W	support indi Section 4.1 The 'm' bits The 'A' bit s The 'i' bits s The 'i' bits s The 'j' bits s 1 1 w4*w4, A, [ Before	irect and reg 14.1 "MAC F s select the o selects the ac select the pr select the the Wy select the Wy [w8]+=2, [w	gister offset a Prefetches". Operand regis ccumulator for refetch differo x prefetch op y prefetch op	addressing as ster Wm for the for the result. ence Wxd de peration. beration. ; Square ; [w8]-[ ; Post-i ; Post-d After	s described in the square. estination. w10] to ACCA w10] to W4 increment W8 decrement W1	1 A 3
Cycles:	_	support indi Section 4.1 The 'm' bits The 'A' bit s The 'i' bits s The 'j' bits s 1 1 v4*W4, A, [ Before Instruction	irect and reg <b>14.1 "MAC F</b> is select the o selects the ac select the pr select the Wy select the Wy [w8]+=2, [w	jister offset a <b>Prefetches</b> ". operand regis ccumulator for refetch differon x prefetch op y prefetch op (10]-=2, W4	addressing as ster Wm for the or the result. ence Wxd de peration. peration. ; [w8]-[ ; Post-i ; Post-d After Instruct	s described in he square. estination. w10] to W4 increment W8 decrement W1 r	1 A 3
Cycles:	W4	support indi Section 4.1 The 'm' bits The 'A' bit s The 'i' bits s The 'j' bits s 1 1 w4*W4, A, [ Before Instruction 0	irect and reg 14.1 "MAC F s select the o selects the ac select the pr select the the Wy select the Wy [w8]+=2, [w	<pre>ister offset a Prefetches". operand regis ccumulator for refetch differon x prefetch op y prefetch op (10]-=2, W4</pre>	addressing as ster Wm for the or the result. ence Wxd de peration. peration. ; [w8]-[ ; Post-d ; Post-d After Instruct	s described in he square. estination. w10] to W4 increment W8 decrement W1 r tion 0057	1 A 3
Cycles:	_	support indi Section 4.1 The 'm' bits The 'A' bit s The 'i' bits s The 'j' bits s 1 1 w4*w4, A, [ Before Instruction 0	irect and reg <b>14.1 "MAC F</b> is select the o selects the ac select the pr select the Wy select the Wy [W8]+=2, [W n 109A	jister offset a <b>Prefetches</b> ". operand regis ccumulator for refetch differon x prefetch op y prefetch op (10]-=2, W4	addressing as ster Wm for the result. ence Wxd de peration. beration. ; Square ; [W8]-[ ; Post-i ; Post-i ; Post-d After	s described in he square. estination. w10] to W4 increment W8 decrement W1 r	1 A 3
Cycles: <u>Example 1:</u>	W4 W8	support indi Section 4.1 The 'm' bits The 'A' bit s The 'i' bits s The 'j' bits s 1 1 w4*w4, A, [ Before Instruction 0	irect and reg <b>14.1 "MAC F</b> is select the o selects the ac select the pr select the Wy select the Wy [w8]+=2, [w n 109A 1100 2300	yister offset a <b>Prefetches</b> ". operand regis ccumulator for refetch differon x prefetch op y prefetch op 110]-=2, W4 W4 W8	addressing as ster Wm for the result. ence Wxd de peration. peration. ; Square ; [w8]-[ ; Post-i ; Post-d After Instruct	s described in he square. estination. estination. w10] to W4 increment W8 decrement W1 r ion 0057 1102 22FE	1 4 3
Cycles: Example 1:	W4 W8 W10	support indi Section 4.1 The 'm' bits The 'A' bit s The 'i' bits s The 'j' bits s 1 1 v4*W4, A, [ Before Instruction 0 1 2 00 3D0A 0	irect and reg <b>14.1 "MAC F</b> is select the o selects the ac select the pr select the Wy select the Wy [w8]+=2, [w n 109A 1100 2300	yister offset a <b>Prefetches</b> ". operand regis ccumulator for refetch differon x prefetch op y prefetch op (10]-=2, W4 W4 W8 W10	addressing as ster Wm for the or the result. ence Wxd de peration. peration. ; [w8]-[ ; Post-i ; Post-d After Instruct	s described in he square. estination. estination. w10] to W4 increment W8 decrement W1 r ion 0057 1102 22FE	1 4 3
Cycles: Example 1:	W4 W8 W10 ACCA	support indi Section 4.1 The 'm' bits The 'A' bit s The 'i' bits s The 'j' bits s 1 1 w4*W4, A, [ Before Instruction 0 1 2 00 3D0A 0 0 0	irect and reg <b>14.1 "MAC F</b> is select the o selects the ac select the pr select the Wy select the Wy [W8]+=2, [W n 109A 1100 2300 1000	yister offset a <b>Prefetches</b> ". operand regis ccumulator for refetch differon x prefetch op y prefetch op (10]-=2, W4 W4 W8 W10 ACCA	addressing as ster Wm for the or the result. ence Wxd de peration. peration. ; Square ; [w8]-[ ; Post-d After Instruct 00 00000	s described in he square. estination. estination. w10] to W4 increment W8 decrement W1 r tion 0057 1102 22FE 5CA4	1 4 3

Example 2: ED W5\*W5, B, [W9]+=2, [W11+W12], W5 ; Square W5 to ACCB

; [W9]-[W11+W12] to W5 ; Post-increment W9

	Before
	Instruction
W5	43C2
W9	1200
W11	2500
W12	8000
ACCB	00 28E3 F14C
Data 1200	6A7C
Data 2508	2B3D
SR	0000

	After Instruction					
W5	3F3F					
W9	1202					
W11	2500					
W12	0008					
ACCB	00 11EF 1F04					
Data 1200	6A7C					
Data 2508	2B3D					
SR	0000					

EDAC		D100.45	<b>D</b>   <b>D</b>   <b>U</b>   <b>U</b>	<b>B</b> 100.45					
Implemented in	1:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
					Х	Х	Х		
Syntax: {	label:}	EDAC	Wm * Wm,	Acc.	[Wx],	[Wy],	Wxd		
			,	, 100,		[Wy] + = ky,	· · · · ·		
					kx,	[]			
					[Wx] - = kx,	[Wy] – = ky,			
					[W9 +	[W11 +			
					W12],	W12],			
Operands:		Wm * Wm ∈ Wx ∈ [W8, '	Acc $\in$ [A,B] Wm * Wm $\in$ [W4 * W4, W5 * W5, W6 * W6, W7 * W7] Wx $\in$ [W8, W9]; kx $\in$ [-6, -4, -2, 2, 4, 6] Wy $\in$ [W10, W11]; ky $\in$ [-6, -4, -2, 2, 4, 6] Wxd $\in$ [W4 W7]						
Operation:		(Acc(A or B	)) + (Wm) * (	(Wm) →Aco	c(A or B)				
		([Wx] – [Wy							
		(Wx) + kx – (Wy) + ky –							
Status Affected	:	( ), )	AB, SA, SB,	SAB					
Encoding:		1111	00mm	A1xx	00ii	iijj	jj10		
Description:				Wm, and a	lso the differe	ence of the pro			
		results of [V Operands V support indi	Vx] – [Wy] ar Vx, Wxd and	e stored in Wyd spec jister offset	Wxd, which i ify the prefet addressing a	ified accumula may be the sa ch operations as described ir	me as Wrr which		
Words:		The 'A' bit s The 'x' bits s The 'i' bits s	elects the ad	ccumulator efetch diffe x prefetch c	•				
Cycles:		1							
Example 1:	EDAC	- W4*W4, A,	[W8]+=2,	[w10]-=2,	; a ; [ ; F	Gquare W4 an Idd to ACCA [W8]-[W10] t Post-increme Post-decremen	o W4 nt W8		
		Before			After				
	F	Instructio			Instruct				
	W4		A600	W4		0057			
	W8		1100	W8		1102			
	W10		2300	W10		22FE			
Data 1	CCA	00 3D0A 3		ACCA					
Data 2			007F 0028	Data 1100 Data 2300		007F 0028			
	SR		0028	SR		0028			
			5500	36		3000			

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Instruction Descriptions Example 2: EDAC W5\*W5, B, [w9]+=2, [W11+W12], W5

; Square W5 and

; add to ACCB

; [W9]-[W11+W12] to W5

; Post-increment W9

	Before Instruction					
W5	43C2					
W9	1200					
W11	2500					
W12	8000					
ACCB	00 28E3 F14C					
Data 1200	6A7C					
Data 2508	2B3D					
SR	0000					

	After
	Instruction
W5	3F3F
W9	1202
W11	2500
W12	8000
ACCB	00 3AD3 1050
Data 1200	6A7C
Data 2508	2B3D
SR	0000

# **Section 5. Instruction Descriptions**

EXCH	Exchange Wns and Wnd						
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	EXCH	Wns,	Wnd			
Operands:	Wns $\in$ [W0 Wnd $\in$ [W0						
Operation:	(Wns) $\leftrightarrow$ (V	Vnd)					
Status Affected:	None						
Encoding:	1111	1101	0000	0ddd	d000	SSSS	
Description:		he word cont must be used			ers. Register	direct	
	The 's' bits	select the ad select the ad	dress of the s	second regist			
Words:	Note:	This instruction	on only exect	utes in Word	mode.		
Cycles:	1						
Cycles.	1						
Example 1: EX	CH W1, W9	; Excha	nge the co	ntents of W	1 and W9		
	Before		Af				
	Instruction		Instru				
W1 W9				43A3 55FF			
SF				0000			
Example 2: EX	CH W4, W5	; Excha	inge the co	ntents of W	4 and W5		
Example 2: EX	Before		Af	er	4 and W5		
	Before Instruction	I	Af	er	4 and W5		
Example 2: EX	Before Instruction	)	Afi Instru W4	er	4 and W5		

FBCL	Find First Bit Change from Left								
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	FBCL	Ws, [Ws], [Ws++], [Ws], [++Ws],	Wnd					
			[Ws],						
Operands:	$Ws \in [W0]$ Wnd $\in [W0]$								
Operation:	Sign = (Ws Temp = (W Shift = 0 While ( (Sh Temp = <sup>-</sup>	While ( (Shift < Max_Shift) && ( (Temp & 0x8000) == Sign) ) Temp = Temp << 1 Shift = Shift + 1							
Status Affected:	С								
Encoding:	1101	1111	0000	0ddd	dppp	SSSS			
Description:	negative va Ws and wo	llue), starting rking towards	from the Mo the Least Si	a positive va st Significant gnificant bit of 16 bits and p	bit after the f the word op	sign bit of berand. The			
	The next Most Significant bit after the sign bit is allocated bit number 0 and the Least Significant bit is allocated bit number -14. This bit ordering allows for the immediate use of Wd with the SFTAC instruction for scaling values up. If a bit change is not found, a result of -15 is returned and the C flag is set. When a bit change is found, the C flag is cleared.								
	flag is set.	When a bit ch	lange is loun	u, the C hay	is cleared.				
	The 'd' bits The 'p' bits	When a bit ch select the de select the so select the so	stination regi urce Address	ister. s mode.					
	The 'd' bits The 'p' bits The 's' bits	select the de select the so select the so	stination regi urce Address urce register.	ister. s mode.					
Words:	The 'd' bits The 'p' bits The 's' bits	select the de select the so select the so	stination regi urce Address urce register.	ister. s mode.					

Note 1: In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1:	FBCL W1, W9	; Find 1st bit change from left in W1 ; and store result to W9
	Before Instruction W1 55FF W9 FFFF SR 0000	After Instruction W1 55FF W9 0000 SR 0000
Example 2:	FBCL W1, W9	; Find 1st bit change from left in W1 ; and store result to W9
	Before Instruction W1 FFFF W9 BBBB SR 0000	After Instruction W1 FFFF W9 FFF1 SR 0001 (C = 1)
Example 3:	FBCL [W1++], W9	; Find 1st bit change from left in [W1] ; and store result to W9 ; Post-increment W1
Data	Before Instruction W1 2000 W9 BBBB 2000 FF0A SR 0000	After Instruction W1 2002 W9 FFF9 Data 2000 FF0A SR 0000

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
implemented in.	X	X	X	X	X	X		
Syntax:	{label:}	FF1L	Ws,	Wnd		1		
			[Ws], [Ws++],					
			[WS],					
			[++Ws],					
			[Ws],					
Operands:	Ws $\in$ [W0 Wnd $\subset$ [W(	-						
Operation: Status Affected: Encoding:	Max_Shift Temp = (W Shift = 1 While ( (Shift = 1 Shift = S If (Shift == $0 \rightarrow$ (Wn Else Shift $\rightarrow$ (Wn C	While ( (Shift < Max_Shift) && !(Temp & 0x8000) ) Temp = Temp << 1 Shift = Shift + 1 If (Shift == Max_Shift) 0 ->(Wnd) Else Shift ->(Wnd)						
Description:	Ws and wo	1100111110000ddddpppssssFinds the first occurrence of a '1' starting from the Most Significant bit of Ws and working towards the Least Significant bit of the word operand. The bit number result is zero-extended to 16 bits and placed in Wnd.						
	Bit numbering begins with the Most Significant bit (allocated number 1) and advances to the Least Significant bit (allocated number 16). A result of zero indicates a '1' was not found, and the C flag will be set. If a '1' is found, the C flag is cleared.							
	ister. s mode.							
	Note:	This instructi	on operates i	in Word mode	e only.			
Words:	1							
Cycles:	1 <sup>(1)</sup>							

**Note 1:** In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see **Note 3** in **Section 3.2.1** "Multi-Cycle Instructions".

Example 1: FF1L W2, W5 ; Find the 1st one from the left in W2 ; and store result to W5 After Before Instruction Instruction 000A 000A W2 W2 000D W5 BBBB W5 SR 0000 SR 0000 FF1L [W2++], W5 ; Find the 1st one from the left in [W2] Example 2: ; and store the result to  $\ensuremath{\mathsf{W5}}$ ; Post-increment W2 Before After Instruction Instruction W2 2000 2002 W2 W5 BBBB W5 0000 0000 Data 2000 0000 Data 2000 0000 0001 (C = 1) SR SR

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
·	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	FF1R	Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws],	Wnd					
Operands:	Ws∈[W0 Wnd∈[W0								
Operation:	Max_Shift : Temp = (W Shift = 1 While ( (Sh Temp = Shift = S If (Shift ==	While ( (Shift < Max_Shift) && !(Temp & 0x1) ) Temp = Temp >> 1 Shift = Shift + 1 If (Shift == Max_Shift) 0 →(Wnd) Else							
Status Affected:	С								
Encoding:	1100	1111	0000	0ddd	dppp	SSSS			
Description:	Ws and wo	rking towards	s the Most Sig	rting from the gnificant bit of 16 bits and p	the word op	erand. The			
	Bit numbering begins with the Least Significant bit (allocated number 1) and advances to the Most Significant bit (allocated number 16). A result of zero indicates a '1' was not found, and the C flag will be set. If a '1' is found, the C flag is cleared.								
	The 'p' bits	select the de select the so select the so	urce Address	s mode.					
	Note:	This instructi	on operates i	in Word mode	e only.				
Words:	1								
Cycles:	1(1)								

Note 1: In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1: FF1R W1, W9 ; Find the 1st one from the right in W1 ; and store the result to W9  $\,$ After Before Instruction Instruction 000A 000A W1 W1 0002 W9 BBBB W9 SR 0000 SR 0000 ; Find the 1st one from the right in [W1] Example 2: FF1R [W1++], W9 ; and store the result to  $\ensuremath{\texttt{W9}}$ ; Post-increment W1 After Before Instruction Instruction W1 2000 2002 W1 0010

W9

SR

Data 2000

8000

0000

W9

SR

Data 2000

BBBB

8000

0000

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GOTO		Unconditi	onal Jum	p			
Implemented in:	PIC24F	PIC24H	PIC2	4E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х		Х	Х	Х
Syntax:	{label:}	GOTO	Expr				
Operands:	Expr may b Expr is reso				ot a literal). where lit23 ∈	= [0 83886	D6].
Operation:	lit23 →PC N0P →Instr	uction Regi	ster				
Status Affected:	None						
Encoding:							
1st word	0000	0100	nnr	n	nnnn	nnnn	nnn0
2nd word	0000	0000	000	0	0000	0nnn	nnnn
Description:	memory rar	nge. The PC Since the F ignored.	C is loaded C must al	with ways	the 4M instru the 23-bit liter reside on an o	al specified i	n the
		The linker v used.	vill resolve	the s	pecified expre	ession into th	e lit23 to be
Words:	2						
Cycles:	2 (PIC24F, 4 (PIC24E,			sPIC3	3F)		
Example 1:	026000 026004	GOTO MOV	_THERE W0, W1		; Jı	ump to _THE	RE
	027844 _THE 027846		#0x400,	w2	,	ode executi esumes here	on
	Befor Instruct PC 02 6 SR 0	ion		PC SR	After Instruction 02 7844 0000		
Example 2:	000100 _code 026000 026004	e:  GOTO 	_code+2			art of code mp to _code	
	Before Instructi PC 02.60	e on		PC SR	After Instruction 00 0102 0000		

GOTO		Unconditio	nal Indirect	Jump		
Implemented in	: PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х		Х		Х
Syntax:	{label:}	GOTO	Wn			
Operands:	Wn∈ [W0	W15]				
Operation:	0 →PC<02	>) →PC<15:1:				
Status Affected	: None					
Encoding:	0000	0001	0100	0000	0000	SSSS
	into PC<1 boundary,	ded into PC< 5:1>. Since th Wn<0> is ign	e PC must al ored.	ways reside (		
Words:	1 ne 's' bits	s select the so	urce register.			
Cycles:	2					
Cycles.	2					
Example 1:	006000 006002		1), W1	,	np uncondit 16-bit val	
	007844 _THER 007846	E: MOV #0>	400, W2	,	de executio sumes here	n
	Before Instructio W4 78 PC 00 60 SR 00	44 00	W4 PC SR	After Instruction 7844 00 7844 0000		

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GOTO		Unconditio	nal Indirect	Jump			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
			Х			Х	
Syntax:	{label:}	GOTO	Wn				
Operands:	Wn∈[W0	) W15]					
Operation:	0 →PC<0	>) →PC<15:1					
Status Affected:	None						
Encoding:	0000	0001	0000	0100	0000	SSSS	
Description:	Zero is loa into PC<1 boundary,	aded into PC< 5:1>. Since th Wn<0> is ign	22:16> and the PC must all ored.	ne value spec ways reside o	cified in (Wn)	is loaded	
Words:	1	s select the so	burce register.				
Cycles:	4						
Cycles.	4						
Example 1:	006000 006002	GOTO ₩4 MOV ₩0	4 9, W1		np uncondit 16-bit val		
	007844 _THER 007846	E: MOV #0:	×400, W2	,	de executio sumes here	n	
	Before Instruction W4 78 PC 00 60 SR 00	44 00	W4 PC SR	After Instruction 7844 00 7844 0000			
GOTO.L		Unconditior	nal Indirect .	Jump Long			
-------------------------	-------------------------------------	---	-------------------------	------------------------------	--------------	----------	--
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
			Х			Х	
Syntax:	{label:}	GOTO.L	Wn				
Operands:	Wn ∈ [W0,	Wn ∈ [W0, W2, W4, W6, W8, W10, W12]					
Operation:	PC<23> → PC<15:0>r	PC<23> (see	text); (Wn+1	)<6:0> →₽C·	<22:16>; (Wr	ו) →	
Status Affected:	None						
Encoding:	0000	0001	1www	w100	0000	SSSS	
Description:	Uncondition	nal indirect jur	mp to any us	er program n	nemory addre	ess.	
	(Wn) is load PC<23> is	The LS 7-bits of (Wn+1) are loaded in PC<22:16>, and the 16-bit value (Wn) is loaded into PC<15:0>. PC<23> is not modified by this instruction. The contents of (Wn+1)<15:7> are ignored.					
	The value of GOTO is a The 's' bits	of Wn<0> is a two-cycle ins select the ad specify the a	lso ignored a truction.	and PC<0> is Wn source re	egister.	0 0.	
Words:	1						
Cycles:	4						
Example 1: 0260 0260		GOTO.L W4 MOV W0, 	W1	; Cal	l _FIR subr	routine	
026) 026)	844 _FIR: 846	MOV #0x4	100, W2	; _FI	R subroutir	ne start	
	Before			After			
	Instruction	-		nstruction			
PC	02 6000		PC	02 6844			
W4	6844		W4	6844			
W5 W15	0002 A268		W5 W15	0002			
Data A268	FFFF		ata A268	A26C 6004			
Data A26A	FFFF		ata A26A	0004			
SR	0000	_	SR	0000			

INC		Increment f				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	INC{.B}	f	{,WREG}		
Operands:	f∈ [0 81	91]				
Operation:	(f) + 1 →de	stination desi	gnated by D			
Status Affected:	DC, N, OV,	Z, C				
Encoding:	1110	1100	0BDf	ffff	ffff	ffff
Description:	destination destination	o the contents register. The register. If When the tent of ten	he optional REG is spec	WREG op ified, the res	erand deter ult is stored i	mines the
	The 'D' bit	selects byte o selects the de select the ado	estination ('0'	for WREG, "		
	<b>Note 1:</b> The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a .W extension to denote a word operation, but it is not required.					
Mordo		The WREG is	Set to working	ng register w	0.	
Words: Cycles:	1 1 <sup>(1)</sup>					
read-mo details, s	dify-write ope	24E devices, erations on no Section 3.2.1	n-CPU Speci 1 "Multi-Cyc	al Function F	egisters. For ns".	
Data 1000		Data 10	After Instruction 00 8F00 SR 0101	n (DC, C = 1)		
Example 2: IN	C 0x1000,	,	ncrement 0: Word mode)	x1000 and s	tore to WRE	ĒĠ
WREG Data 1000		WRE Data 100		I		

INC		Increment V	Ns			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	INC{.B}	Ws,	Wd		
			[Ws],	[Wd]		
			[Ws++],	[Wd++]		
			[Ws],	[Wd]		
			[++Ws],	[++Wd]		
			[Ws],	[Wd]		
Operands:	$\begin{array}{l} Ws \in [W0 \\ Wd \in [W0 \end{array}$					
Operation:	(Ws) + 1 –	→Wd				
Status Affected:	DC, N, OV,	, Z, C				
Encoding:	1110	1000	0Bqq	qddd	dppp	SSSS
Description:		ne contents of n register Wd. /s and Wd.				
	The 'q' bits The 'd' bits The 'p' bits	selects byte o s select the de s select the de s select the so s select the so	estination Add estination regi ource Address	dress mode. ister. s mode.	ord, '1' for uy	/te).
	Note:	rather than a	a word operat	instruction de tion. You may but it is not re	yusea.We	
Words:	1				•	
Cycles:	1 <sup>(1)</sup>					
read-mo details, s	odify-write op	C24E devices, perations on no n Section 3.2. ++W2]	on-CPU Spec .1 "Multi-Cyc ; Pre-inc	cial Function F cle Instructio crement W2	Registers. For ns".	r more
			; Increme ; (Byte m	ent W1 and s node)	tore to W2	
	Before Instruction		After Instructio	ึงท		

Example 2:	INC W1, W2	; Increment W1 and store to W2 ; (Word mode)
	Before Instruction	After Instruction
	W1 FF7F	W1 FF7F
	W2 2000	W2 FF80
	SR 0000	SR 0108 (DC, N = 1)

## **Section 5. Instruction Descriptions**

Implemented in:						
implementeu m.	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	INC2{.B}	f	{,WREG}		
Operands:	f ∈ [0 81	91]				
Operation:	(f) + 2 →de	stination desi	gnated by D			
Status Affected:	DC, N, OV,	Z, C				
Encoding:	1110	1100	1BDf	ffff	ffff	ffff
Description:	destination destination WREG is n	e contents of register. The register. If W ot specified, t selects byte o	optional WR REG is speci the result is s	EG operand of ified, the result tored in the fi	determines th It is stored in Ie register.	he 1 WREG. If
	The 'D' bit s	selects the de select the add	estination ('0'	for WREG, '1		
		<b>Note:</b> The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a .W extension to denote a word operation, but it is not required.				
Words:	1					
Cycles:	1 <sup>(1)</sup>					
			' '-tad our	· · · · · · · · · · · · · · · · · · ·	t t	
read-mo details, s	odify-write ope		on-CPU Spec	ial Function R cle Instruction	Registers. For	
read-mo details, s	bdify-write ope see Note 3 in C2.B 0x106 Before Instruction D 8FFF R 0000	erations on no <b>Section 3.2.</b> 90 ; Incre ; (Byte Data 10	on-CPU Spec <b>1 "Multi-Cyc</b> ement 0x100 e mode) After Instruction 000 8F01 SR 0101	ial Function R cle Instruction 0 by 2 n	Registers. For <b>ns</b> ".	r more

INC2		Increment \	Ns by 2			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	INC2{.B}	Ws,	Wd		
			[Ws],	[Wd]		
			[Ws++],	[Wd++]		
			[Ws],	[Wd]		
			[++Ws],	[++Wd]		
			[Ws],	[Wd]		
Operands:	Ws ∈ [W0 . Wd ∈ [W0					
Operation:	(Ws) + 2 →	Wd				
Status Affected:	DC, N, OV,	Z, C	-			-
Encoding:	1110	1000	1Bqq	qddd	dppp	SSSS
Description:		register Wd.		gister Ws and ct or indirect a		
	The 'q' bits The 'd' bits The 'p' bits	select the de select the de	stination Add stination regi urce Address	ster.	ord, '1' for byt	e).
		rather than a	a word opera	instruction de tion. You may out it is not ree	use a .W e	
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-m details	nodify-write o	perations on r in <b>Section 3.</b> [++W2] ;	non-CPU Spe 2.1 "Multi-Cy Pre-increm		Registers. For ns".	
			Increment (Byte mode	by 2 and sto )	ore to W1	
W Data 200	Before Instruction /1 FF7F /2 2000 00 ABCD GR 0000	Data 2	After Instruction W1 FF7F W2 2001 2000 81CD SR 0100		r = 1)	

Example 2:	INC2 W1, W2	; Increment W1 by 2 and store to W2 ; (word mode)
	Before Instruction	After Instruction
	W1 FF7F	W1 FF7F
	W2 2000	W2 FF81
	SR 0000	SR 0108 (DC, N = 1)

Instruction Descriptions

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Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	IOR{.B}	f	{,WREG}		
Operands:	f ∈ [0 81	.91]				
Operation:	(f).IOR.(W	REG) →destir	nation design	ated by D		
Status Affected:	N, Z					
Encoding:	1011	0111	0BDf	ffff	ffff	ffff
	the destination destination WREG is r	REG and the cation register. To register. If W not specified, to a specified, to a specified, to a specified of the specified	The optional REG is spec the result is s	WREG operative operation with the second sec	and determin ult is stored in ile register.	nes the n WREG. If
	The 'D' bit	selects byte o selects the de select the add	estination ('0'	for WREG, "		
		The extension rather than a denote a work The WREG is	word operati d operation,	on. You may but it is not re	use a .W ext equired.	•
Words:	<b>2</b> . 1			ng register w	10.	
Cycles:	1 <sup>(1)</sup>					
read-mo details, s	dify-write op		on-CPU Spec 1 "Multi-Cyc	ial Function F	Registers. Foi ns".	
	Before		After			
	Instruction		Instructio	n		
WREG		WRE				
Data 1000 SR		Data 10	00 FF34 SR 0000			
Example 2: 10F	R 0x1000,		DR (0x1000) Word mode)	to WREG		
	Before Instruction		After Instructio	n		
WREG		WRE		-		
Data 1000	0FAB	Data 10	00 OFAB			

0008 (N = 1)

SR

SR

		Inclusive O	R Literal and	l Wn		
Implemented in:		PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	IOR{.B}	#lit10,	Wn		
Operands:	lit10 ∈ [0	lit10 $\in$ [0 255] for byte operation lit10 $\in$ [0 1023] for word operation Wn $\in$ [W0 W15]				
Operation:	lit10.IOR.(\					
Status Affected:		·		_	_	
Encoding:	1011	0011	0Bkk	kkkk	kkkk	dddd
Description:	and the co	Compute the logical inclusive OR operation of the 10-bit literal operand and the contents of the working register Wn and place the result back into the working register Wn.				
	The 'k' bits	The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'k' bits specify the literal operand. The 'd' bits select the address of the working register.				∕te).
	2:	The extension rather than a denote a word For byte oper- unsigned valu <b>Operands</b> " for Byte mode.	word operation d operation, k rations, the lite ue [0:255]. Se	on. You may but it is not re teral must be ee <b>Section 4.</b>	use a .W exte equired. specified as .6 "Using 10	an <b>-bit Literal</b>
Words:	1					
Cycles:	1					
Example 1:	IOR.B #0xAA,	,	IOR 0xAA to (Byte mode)			
	Before Instruction W9 1234 SR 0000		After Instruction W9 12BE SR 0008	]		
Example 2:	IOR #0x2AA,		IOR 0x2AA to (Word mode)			
	Before Instruction W4 A34D SR 0000		After Instruction W4 A3EF SR 0008	]		

IOR			R Wb and S		1	1
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	X
Syntax:	{label:}	IOR{.B}	Wb,	#lit5,	Wd	
					[Wd]	
					[Wd++]	
					[Wd]	
					[++Wd]	
					[Wd]	
Operands:	Wb∈ [W0	W15]				
•	lit5 ∈ [0	31]				
	$Wd \in W0$	-				
Operation:	(Wb).IOR.I	t5 →Wd				
Status Affected:	N, Z			1		-
Encoding:	0111	0www	wBqq	qddd	d11k	kkkk
Description:		ne logical incl				
		and the 5-bi register Wd.				
		ster direct or i	0		0	
	-	select the ac				
		selects byte c				/te).
		select the de				
		select the de provide the li	•		teger numbei	r.
	Note:	The extension				
		rather than a denote a wor			-	extension to
Words:	1		<b>1</b> ,		•	
Cycles:	1					
Example 1:	OR.B W1, #	0×5, [W9++]	; IOR W1	and 0x5 (B	yte mode)	
			; Store t			
			; Post-ir	ncrement W9		
	Before		After			
	Instruction		Instructio	-		
	V1 AAAA		W1 AAAA			
	V9 2000		W9 2001			
Data 20	00 0000 SR 0000	Data 2	000 00AF SR 0008			
	5K 0000		SK 0000			
Example 2:	IOR W1, #0x		IOR W1 with Store to W9	n 0x0 (Word 9	mode)	
	Before		After			
				-		
	V1 0000 V9 A34D		W1 0000 W9 0000			
	V9 A34D SR 0000		W9 0000 SR 0002			
				_ (~)		

IOR		1		-		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	IOR{.B}	Wb,	Ws,	Wd	
2				[Ws],	[Wd]	
				[Ws++],	[Wd++]	
				[Ws],	[Wd]	
				[++Ws],	[++Wd]	
				[Ws],	[Wd]	
Operands:	Wb ∈ [W0 Ws ∈ [W0 Wd ∈ [W0	. W15]				
Operation:	(Wb).IOR.(V	- Vs) →Wd				
Status Affected:	N, Z	-				
Encoding:	0111	0www	wBqq	qddd	dppp	SSSS
	The 'w' bits The 'B' bit s The 'q' bits s The 'd' bits s The 'p' bits s	select the a elects byte c select the de select the de select the so	ddress of the	ister. s mode.	er.	
	Note:	The extension ather than a	on . B in the a word opera	instruction o ation. You ma but it is not re	ay use a .W	
Words:	1		•		•	
Cycles:	1 <sup>(1)</sup>					
read-m details	IC33E and PIC nodify-write op , see <b>Note 3</b> in OR.B W1, ['	erations on r n <b>Section 3.</b> 2	non-CPU Spe 2.1 "Multi-Cy ++] ; IOR ; Stor	cial Function	Registers. Foons".	or more
	Before		After			
W	Instruction /1 AAAA /5 2000 /9 2400 00 1155	Data 2 Data 2	Instruct W1 AAA/ W5 200 W9 240 2000 115	ion A 1 5		

Instruction Descriptions

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Example 2:	IOR W1, W5, W9	; IOR W1 and W5 (Word mode) ; Store the result to W9
	Before	After
	Instruction	Instruction
	W1 AAAA	W1 AAAA
	W5 5555	W5 5555
	W9 A34D	W9 FFFF
	SR 0000	SR 0008 (N = 1)

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
·				Х	Х	Х
Syntax:	{label:}	LAC	Ws,	{#Slit4,}	Acc	
			[Ws],			
			[Ws++],			
			[Ws],			
			[Ws],			
			[++Ws],			
			[Ws+Wb],			
Operands:	Ws ∈ [W0 Wb ∈ [W0 Slit4 ∈ [-8 Acc ∈ [A,E	W15] +7]				
Operation:	Shift <sub>Slit4</sub> (E	xtend(Ws)) →	Acc(A or B)			
Status Affected:	OA, OB, C	AB, SA, SB, S	SAB			
Encoding:	1100	1010	Awww	wrrr	rggg	SSSS
Description:	shift and s where a ne operand ir register is	contents of the tore the result egative operan idicates an arit assumed to be ded (through b	in the specifie d indicates ar hmetic right s e 1.15 fraction	d accumulato n arithmetic le hift. The data al data and is	r. The shift rai ft shift and a p stored in the automatically	nge is -8:7, positive source
	The 'w' bit The 'r' bits The 'g' bits	specifies the c s specify the o encode the a s select the so s specify the so	ffset register v ccumulator pr urce Address	Wb. e-shift. mode.		
	Note:	upper Accum	ulator registe	ore than sign r (AccxU), or aturation bits	causes a sat	
Words:	1					

details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

# **16-bit MCU and DSC Programmer's Reference Manual**

Example 1: LAC	[W4++], #-3, B	; Contents of ; Post increm	vith [W4] << 3 [W4] do not c ment W4 mation disable	C C
	Before		After	
	Instruction		Instruction	
W4	2000	W4	2002	
ACCB	00 5125 ABCD	ACCB	FF 9108 0000	
Data 2000	1221	Data 2000	1221	
SR	0000	SR	4800	(OB, OAB = 1)
Example 2: LAC	[W2], #7, A			Ũ
	Before		After	
	Instruction		Instruction	
W2	4002	W2	4000	
ACCA	00 5125 ABCD	ACCA	FF FF22 1000	
Data 4000	9108	Data 4000	9108	
Data 4002	1221	Data 4002	1221	
SR	0000	SR	0000	

#### **Section 5. Instruction Descriptions**

LNK		Allocate Sta	ack Frame			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х		Х	Х	
Syntax:	{label:}	LNK	#lit14			
Operands:	lit14 ∈ [0	. 16382]				
Operation:	(W14) →(T (W15) + 2 (W15) →W (W15) + lit	→W15 /14				
Status Affected:	None					
Encoding:	1111	1010	00kk	kkkk	kkkk	kkk0
Description:	subroutine the conten updated St the Stack F	ction allocates calling seque ts of the Fran ack Pointer (\ Pointer by the maximum Sta	ence. The Sta ne Pointer (W N15) to the F unsigned 14	ack Frame is /14) onto the rame Pointer -bit literal op	allocated by stack, storin r and then inc erand. This in	PUSHing g the crementing
	The 'k' bits	specify the s	ize of the Sta	ack Frame.		
	Note:	Since the St lit14 must be		can only resid	de on a word	d boundary
Words:	1					
Cycles:	1					
Example 1: LNK	#0xA0	; Allocate	a stack fra	ame of 160	bytes	
	Befor			After		
\A/A A	Instruct		14/1 4	Instructio		
W14		2000	W14		2002	

W15

SR

Data 2000

20A2

2000

0000

5

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W15

SR

Data 2000

2000

0000

. . . . . .

W14

W15

SR

Data 2000

CORCON

2000

2000

0000

0000

0000

LNK		Allocate Sta	ack Frame			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	LNK	#lit14			
Operands:	lit14 ∈ [0 .	. 16382]				
Operation:	(W14) →(T (W15) + 2 (W15) →M 1 →SFA bi (W15) + lit	→W15 /14 t				
Status Affected:	SFA					
Encoding:	1111	1010	00kk	kkkk	kkkk	kkk0
Description:	subroutine the conten updated Si the Stack I	ction allocates calling seque ts of the Fram ack Pointer (N Pointer by the maximum Sta	ence. The Sta ne Pointer (W W15) to the F unsigned 14	ack Frame is /14) onto the rame Pointe -bit literal op	allocated by stack, storin r and then in erand. This i	PUSHing g the crementing
	The 'k' bits	specify the s	ize of the Sta	ick Frame.		
	Note:	Since the Sta lit14 must be		can only resi	de on a word	d boundary
Words:	1					
Cycles:	1					
Example 1: LN	K #0xA0	; Allocate	a stack fra	ame of 160	bytes	
	Befor	e		After		
	Instruct	-		Instructio	n	

W14

W15

SR

Data 2000

CORCON

2002

20A2

2000

0000

LSR		Logical Shif	it Right f			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	LSR{.B}	f	{,WREG}		
Operands:	f ∈ [0 81	91]				
Operation:	(f<0>) → For word of 0 →Dest	<7> →Dest<6:0> C <u>oeration:</u> <15> ) →Dest<14:0 C	>			
	0	►C				
Status Affected:	N, Z, C					
Encoding:	1101	0101	0BDf	ffff	ffff	ffff
Description:	in the desti shifted into Most Signif The optiona is specified	ntents of the f nation register the Carry bit of icant bit of the al WREG open , the result is ired in the file	r. The Least of the STATL destination rand determi stored in WR	Significant bit JS register. Ze register. nes the destir	of the file reg ro is shifted i nation register	ister is nto the r. If WREG
	The 'D' bit	selects byte or selects the de select the add	stination ('0'	for WREG, '1		
		The extension rather than a v denote a word	word operation	on. You may u	se a .W exte	
	2:	The WREG is	set to working	ng register W0	).	
Words:	1					
read-m	nodify-write o	IC24E devices perations on n in <mark>Section 3.2</mark>	ion-CPU Spe	cial Function I	Registers. For	
Example 1: L	SR.B 0x60	9 ; Logica ; (Byte		right (0x60	9) by one	
Data 60 S	Before Instruction 00 55FF 3R 0000	) Data	After Instructi 600 557F SR 0002	=		

Example 2: LSR

LSR 0x600, WREG ; Logically shift right (0x600) by one ; Store to WREG

```
; (Word mode)
```

I	Before nstruction		After Instructior	า
Data 600	55FF	Data 600	55FF	
WREG	0000	WREG	2AFF	
SR	0000	SR	0001	(C = 1)
-				(C :

Implemented in:		Logical Shi	3			
implementeu in.	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	LSR{.B}	Ws,	Wd		
-		-	[Ws],	[Wd]		
			[Ws++],	[Wd++]		
			[Ws],	[Wd]		
			[++Ws],	[++Wd]		
			[Ws],	[Wd]		
Operands:	$Ws \in [W0]$ $Wd \in [W0]$	-				
Operation:	(Ws<0>) <u>For word c</u> 0 →Wd< (Ws<15: (Ws<0>)	<7> →Wd<6:0 ) →C <u>operation:</u> <15> :1>) →Wd<14 ) →C				
	0->	►C				
	N, Z, C	1		· <b>T</b>	r	1
Status Affected: Encoding:	1101	0001	0Bqq	qddd	dppp	SSSS
	1101 Shift the co the result in shifted into Most Signit	ntents of the the destinat the Carry bit	source regis tion register \ t of the STAT Vd. Either reg	qddd ster Ws one bi Wd. The Leas US register. Z gister direct or	it to the right, It Significant I Zero is shifted	, and place bit of Ws is d into the
Encoding:	1101 Shift the cc the result in shifted into Most Signif may be use The 'B' bit : The 'q' bits The 'q' bits The 'd' bits The 'p' bits	ontents of the n the destinat the Carry bit ficant bit of W ed for Ws and	e source regis tion register V t of the STAT Vd. Either reg d Wd. or word opera estination Ad estination reg pource Addres	ster Ws one bi Wd. The Leas US register. Z gister direct or ation ('0' for w dress mode. gister. ss mode.	it to the right, it Significant I Zero is shifted indirect add	, and place bit of Ws is d into the ressing
Encoding:	1101 Shift the cc the result in shifted into Most Signif may be use The 'B' bit : The 'q' bits The 'q' bits The 'd' bits The 'p' bits	pontents of the on the destinat of the Carry bit ficant bit of W ed for Ws and selects byte of select the de select the de select the so select the so The extension rather than a	e source regis tion register V t of the STAT Vd. Either reg d Wd. or word opera estination Ad estination reg ource Addres ource register on .B in the a word opera	ster Ws one bi Wd. The Leas US register. Z gister direct or ation ('0' for w dress mode. gister. ss mode.	it to the right, it Significant I Zero is shifted indirect add vord, '1' for b enotes a byto y use a . W e	, and place bit of Ws is d into the ressing yte).
Encoding:	1101 Shift the co the result ir shifted into Most Signit may be use The 'B' bits The 'q' bits The 'd' bits The 'p' bits The 's' bits	pontents of the on the destinat of the Carry bit ficant bit of W ed for Ws and selects byte of select the de select the de select the so select the so The extension rather than a	e source regis tion register V t of the STAT Vd. Either reg d Wd. or word opera estination Ad estination reg ource Addres ource register on .B in the a word opera	ster Ws one bi Wd. The Leas US register. Z gister direct or ation ('0' for w dress mode. gister. ss mode. r. instruction de ation. You may	it to the right, it Significant I Zero is shifted indirect add vord, '1' for b enotes a byto y use a . W e	, and place bit of Ws is d into the ressing yte).

details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1:	LSR.B W0, W1	; LSR W0 (Byte mode) ; Store result to W1
	Before Instruction W0 FF03 W1 2378 SR 0000	After Instruction W0 FF03 W1 2301 SR 0001 (C = 1)
Example 2:	LSR W0, W1	; LSR W0 (Word mode) ; Store the result to W1
	Before Instruction W0 8000 W1 2378	After Instruction W0 8000 W1 4000

0000

SR

0000

SR

(C = 1)

LSR		Logical Shi	ft Right by S	Short Literal		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	LSR	Wb,	#lit4,	Wnd	
Operands:	Wb ∈ [W0 lit4 ∈ [0 Wnd ∈ [W	15]				
Operation:		→Shift_Val 15:15-Shift_Va iift_Val> <i>→</i> Wn		/al:0>		
Status Affected:	N, Z					
Encoding:	1101	1110	Owww	wddd	d100	kkkk
Description:	unsigned I	ift right the co iteral and stor g must be use	e the result ir	n the destinat		
	The 'd' bits	s select the a s select the de s provide the l	estination reg	jister.	er.	
	Note:	This instructi	on operates	in Word mod	le only.	
Words:	1					
Cycles:	1					
Example 1:	LSR W4, #1		LSR W4 by : Store resu			
	Before Instruction W4 C800 W5 1200 SR 0000	V	After Instruction V4 C800 V5 0003 GR 0000	n   		
Example 2:	LSR W4, #1		LSR W4 by : Store resu			
	Before Instruction W4 0505 W5 F000 SR 0000	V	After Instruction V4 0505 V5 0282 SR 0000			

LSR			Logical Sh	ift Right by \	Wns		
Implemented in	:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
		Х	Х	Х	Х	Х	Х
Syntax:		{label:}	LSR	Wb,	Wns,	Wnd	
Operands:		Wb ∈ [W0 Wns ∈ [W0 Wnd ∈ [W0	)W15]				
Operation:		0 →Wnd<1	→Shift_Val L5:15-Shift_V ift_Val> →Wr	'al + 1> nd<15 - Shift_	_Val:0>		
Status Affected:		N, Z					
Encoding:		1101	1110	0www	wddd	d000	SSSS
Description:		Significant	bits of Wns (	only up to 15	source regis positions) ar ressing must	nd store the r	esult in the
		The 'd' bits	select the de	ddress of the estination reg ource registe		er.	
		Note 1:	This instructi	on operates	in Word mod	e only.	
		2:	If Wns is gre	ater than 15,	Wnd will be	loaded with (	)x0.
Words:		1					
Cycles:		1					
Example 1:	LSR	W0, W1		LSR W0 by N Store resu			
	W0 W1 W2 SR	Before nstruction C00C 0001 2390 0000	V V	After Instruction V0 C00C V1 0001 V2 6006 SR 0000	ı		
Example 2:	LSR	W5, W4		LSR W5 by N Store resu			
		Before struction DD43 000C 0800 0000	V V	After Instruction V3 0000 V4 000C V5 0800 SR 0002	(Z = 1)		

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
				Х	Х	Х
Syntax: {label:}	MAC	Wm*Wn, Acc	{,[Wx], Wxd	}	{,[Wy], Wyd}	{,AWB}
			${,[Wx] + = kx}$	, Wxd}	${,[Wy] + = ky}$	
			${,[Wx] - = k}$		$\{,[Wy] - = ky\}$	
			{,[W9 + W12	2], Wxd}	{,[W11 + W12	2], Wyd}
Operands:	$\begin{array}{l} Acc \in \ [A,B] \\ Wx \in \ [W8, \\ Wy \in \ [W10 \end{array} \end{array}$	[W4 * W5, W4 W9]; kx ∈ [-6, , W11]; ky ∈ [- .3, [W13] + = 2	-4, -2, 2, 4, 6 6, -4, -2, 2, 4	6]; Wxd ∈ [W	/4 W7]	W6 * W7]
Operation:	([Wx]) →W> ([Wy]) →Wy	)) +(Wm) * (Wr kd; (Wx) + kx – rd; (Wy) + ky – )) rounded <i>→</i> A	→Wx →Wy	- В)		
Status Affected:	OA, OB, OA	AB, SA, SB, SA	AB			
Encoding:	1100	Ommm	A0xx	yyii	iijj	jjaa
Description:	in preparation unspecified	contents of tw on for another accumulator r	MAC type ins	truction and	optionally sto	re the
	sign-extend	ed to 40 bits a			l accumulator	
	Operands V which support Section 4.1 store of the	ed to 40 bits a Vx, Wxd, Wy a ort indirect and <b>.4.1 "MAC Pre</b> "other" accum .4.4 "MAC Wr	nd added to nd Wyd spec I register offs f <b>etches</b> ". O ulator, as de	the specified cify optional set addressin perand AWE	l accumulator prefetch opera ig, as describ	ations, ed in
	Operands V which suppo Section 4.1 store of the Section 4.1 The 'm' bits The 'm' bits The 'A' bits The 'A' bits The 'i' bits s The 'i' bits s The 'a' bits Note 1: 1 f 2: 1 0	Vx, Wxd, Wy a ort indirect and 4.1 "MAC Pre "other" accum 4.4 "MAC Wr select the ope elects the accu select the prefe select the prefe select the Wx p select the Wx p select the Wy p select the accu fhe IF bit (COF ractional or an fhe US<1:0> b CON<12> in ds unsigned, signed	nd added to nd Wyd spec I register offs offetches". O ulator, as de ite Back". erand registe umulator for etch Wyd de orefetch oper umulator Wri RCON<0>), o integer. of (CORCO SPIC30F/dsF ed, or mixed-	the specified cify optional set addressir perand AWE scribed in rs Wm and W the result. stination. ation. ation. te Back dest determines if N<13:12> in IC33F) dete	I accumulator prefetch opera g, as describe specifies the Vn for the mu ination. the multiply is dsPIC33E, C rmine if the m	ations, ed in optional Itiply. s OR- ultiply is
Words:	Operands V which suppo Section 4.1 store of the Section 4.1 The 'm' bits The 'm' bits The 'A' bits The 'A' bits The 'i' bits s The 'i' bits s The 'a' bits Note 1: 1 f 2: 1 0	Vx, Wxd, Wy a ort indirect and 4.1 "MAC Pre "other" accum 4.4 "MAC Wr select the ope elects the accus select the pref select the pref select the Wx p select the Wy p select the Wy p select the accus fhe IF bit (COF ractional or an The US<1:0> b CON<12> in ds	nd added to nd Wyd spec I register offs offetches". O ulator, as de ite Back". erand registe umulator for etch Wyd de orefetch oper umulator Wri RCON<0>), o integer. of (CORCO SPIC30F/dsF ed, or mixed-	the specified cify optional set addressir perand AWE scribed in rs Wm and W the result. stination. ation. ation. te Back dest determines if N<13:12> in IC33F) dete	I accumulator prefetch opera g, as describe specifies the Vn for the mu ination. the multiply is dsPIC33E, C rmine if the m	ations, ed in optional Itiply. s OR- ultiply is

....

```
Example 1:
```

- MAC W4\*W5, A, [W8]+=6, W4, [W10]+=2, W5
- ; Multiply W4\*W5 and add to ACCA
- ; Fetch [W8] to W4, Post-increment W8 by 6
- ; Fetch [W10] to W5, Post-increment W10 by 2  $\,$
- ; CORCON = 0x00C0 (fractional multiply, normal saturation)

	Before Instruction		After Instruction
W4	A022	W4	2567
W5	B900	W5	909C
W8	0A00	W8	0A06
W10	1800	W10	1802
ACCA	00 1200 0000	ACCA	00 472D 2400
Data 0A00	2567	Data 0A00	2567
Data 1800	909C	Data 1800	909C
CORCON	00C0	CORCON	00C0
SR	0000	SR	0000

Example 2:

- MAC W4\*W5, A, [W8]-=2, W4, [W10]+=2, W5, W13 ; Multiply W4\*W5 and add to ACCA
- ; Fetch [W8] to W4, Post-decrement W8 by 2
- ; Fetch [W10] to W5, Post-increment W10 by 2
- ; Write Back ACCB to W13
- ; CORCON = 0x00D0 (fractional multiply, super saturation)

	Before Instruction			
W4	1000			
W5	3000			
W8	0A00			
W10	1800			
W13	2000			
ACCA	23 5000 2000			
ACCB	00 0000 8F4C			
Data 0A00	5BBE			
Data 1800	C967			
CORCON	00D0			
SR	0000			

After									
Instruction									
W4	5BBE								
W5	C967								
W8	09FE								
W10	1802								
W13	0001								
ACCA	23 5600 2000								
ACCB	00 0000 1F4C								
Data 0A00	5BBE								
Data 1800	C967								
CORCON	00D0								
SR	8800	(OA, OAB = 1)							

MAC	1	-	d Accumulat		1		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
				Х	Х	Х	
Syntax: {label:}	MAC V	Vm*Wm, Acc	{,[Wx], Wxd	}	{,[Wy], Wyd]	}	
			${,[Wx] + = kx}$	k, Wxd}	{,[Wy] + = k	y, Wyd}	
			{,[Wx] -= k	x, Wxd}	{,[Wy] – = ky	y, Wyd}	
			{,[W9 + W12	2], Wxd}	{,[W11 + W1	.2], Wyd}	
Operands:	$Acc \in [A, E]$ $Wx \in [W8]$	∈ [W4 * W4, ' 8] , W9]; kx ∈ [-6 0, W11]; ky ∈	6, -4, -2, 2, 4,	, 6]; Wxd ∈ [	- W4 W7]	l	
Operation:	$(Acc(A \text{ or } B)) + (Wm) * (Wm) \rightarrow Acc(A \text{ or } B)$ $([Wx]) \rightarrow Wxd; (Wx) + kx \rightarrow Wx$ $([Wy]) \rightarrow Wyd; (Wy) + ky \rightarrow Wy$						
Status Affected:	OA, OB, O	AB, SA, SB, S	SAB				
Encoding:	1111	00mm	A0xx	yyii	iijj	jj00	
Description:	Square the contents of a working register, optionally prefetch operands in preparation for another MAC type instruction. The 32-bit result of the signed multiply is sign-extended to 40 bits and added to the specified accumulator.						
	Operands Wx, Wxd, Wy and Wyd specify optional prefetch operations, which support indirect and register offset addressing, as described in <b>Section 4.14.1 "MAC Prefetches</b> ".						
	The 'A' bit The 'x' bits The 'y' bits The 'i' bits The 'j' bits <b>Note 1:</b>	s select the op selects the ac select the pro- select the pro- select the Wx select the Wy The IF bit (CC	cumulator fo efetch Wxd d efetch Wyd d prefetch op prefetch op ORCON<0>)	r the result. lestination. lestination. eration. eration.		y is frac-	
		tional or an in The US<1:0> CORCON<12 multiply is un devices supp	bits (CORC 2> in dsPIC3 signed, signe	0F/dsPIC33I ed, or mixed-	<ul> <li>determine</li> <li>sign. Only d</li> </ul>	if the	
Words:	1						

```
Example 1:
```

- MAC W4\*W4, B, [W9+W12], W4, [W10]-=2, W5
  - ; Square W4 and add to  $\ensuremath{\mathsf{ACCB}}$
  - ; Fetch [W9+W12] to W4
  - ; Fetch [W10] to W5, Post-decrement W10 by 2
  - ; CORCON = 0x00C0 (fractional multiply, normal saturation)

	Before Instruction		After Instruction
W4	A022	W4	A230
W5	B200	W5	650B
W9	0C00	W9	0C00
W10	1900	W10	18FE
W12	0020	W12	0020
ACCB	00 2000 0000	ACCB	00 67CD 0908
Data 0C20	A230	Data 0C20	A230
Data 1900	650B	Data 1900	650B
CORCON	00C0	CORCON	00C0
SR	0000	SR	0000

Example 2:

MAC W7\*W7, A, [W11]-=2, W7 ; Square W7 and add to ACCA

; Fetch [W11] to W7, Post-decrement W11 by 2

; CORCON = 0x00D0 (fractional multiply, super saturation)

	Before Instruction		After Instruction			
W7	76AE	W7	23FF			
W11	2000	W11	1FFE			
ACCA	FE 9834 4500	ACCA	FF 063E 0188			
Data 2000	23FF	Data 2000	23FF			
CORCON	00D0	CORCON	00D0			
SR	0000	SR	8800	(OA, OAB = 1)		

MOV		Move f to D	estination			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MOV{.B}	f	{,WREG}		
Operands:	f∈ [0 819	91]				
Operation:	(f) →destina	ation designa	ted by D			
Status Affected:	N, Z					
Encoding:	1011	1111	1BDf	ffff	ffff	ffff
Description:	The option WREG is specified, th	ontents of the al WREG of specified, th ne result is st e STATUS re	perand det e result is ored back to	ermines the stored in W	destination /REG. If W	register. If REG is not
	The 'D' bit s	elects byte o selects the de select the add	estination ('0	for WREG,		
	r 2: ⊺ 3: ∖ t	<ul> <li>te 1: The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a . W extension to denote a word operation, but it is not required.</li> <li>2: The WREG is set to working register W0.</li> </ul>				the "MOV f
Words:	1			iaalon rogioto		
Cycles:	1 <sup>(1)</sup>					
<ul> <li>Note 1: In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".</li> <li>Example 1: MOV.B TMR0, WREG ; move (TMR0) to WREG (Byte mode)</li> </ul>						
	Before Instruction		After Instruction			
WREG (W0)	9080	WREG (W0				

	- /	
I WREG (W0) TMR0 SR		After Instruction WREG (W0) 9055 TMR0 2355 SR 0000
Example 2: MOV	0×800	; update SR based on (0x800) (Word mode)
ا Data 0800 SR	Before nstruction B29F 0000	After Instruction Data 0800 B29F SR 0008 (N = 1)

MOV		Move WRE	G to f			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MOV{.B}	WREG,	f		
Operands:	f∈ [0 8	191]				
Operation:	(WREG) –	→f				
Status Affected:	None					
Encoding:	1011	0111	1B1f	ffff	ffff	ffff
Description:		contents of the ile register.	e default wor	king register	WREG into t	he
The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'f' bits select the address of the file register.					yte).	
	Note 1:	The extensio than a word r word move, b	move. You m out it is not re	ay use a .W equired.	extension to	
	2: 3:	The WREG is When moving register mem allows any w ter.	g word data f lory, the "MOV	rom the work / Wns to f	king register a " ( <mark>page 282</mark> )	instruction
Words:	1					
Cycles:	1					
Example 1: M	OV.B WREG,	0×801 ;	move WREG	to 0x801 (	Byte mode)	
WREG (W Data 080 S	·	WREG (\ Data 0	· ·	3		
Example 2: M	OV WREG,	DISICNT	; move WREC	G to DISICN	т	
WREG (W DISICN S		WREG ( DISIO		)		

## **Section 5. Instruction Descriptions**

				<u> </u>		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	X	Х	Х
Syntax:	{label:}	MOV	f,	Wnd		
Operands:	f ∈ [0 65 Wnd ∈ [W0					
Operation:	(f) →Wnd					
Status Affected:	None					
Encoding:	1000	0fff	ffff	ffff	ffff	dddd
	be word-ali	ay reside anyv ligned. Registe select the add s select the de	ter direct addi Idress of the f	lressing must file register.		
	2: 3:	This instruction Since the file upper 15 bits assumed to be To move a by to Destina	e register add s of the file reg be '0'). yte of data fro	lress must be gister addres	e word-aligned ss are encode er memory, th	ed (bit 0 is ne "MOV f
Words:	1				-	
Cycles:	1 <sup>(1)</sup>					
read-mod details, se <u>Example 1:</u> Mov	lify-write ope ee <b>Note 3</b> in	W2 CORCC	move CORCOM After Instruction	ial Function R <b>cle Instructio</b> N to W12 n	Registers. For	
Example 2: MOV	0x27FE	:,W3 ;m	nove (0x27FE	E) to W3		
l W3 Data 27FE	Before Instruction 0035 ABCD	Data 27F	After Instruction W3 ABCD FE ABCD SR 0000	n   		

MOV		Move Wns t	to f			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MOV	Wns,	f		
Operands:	f ∈ [0 65 Wns ∈ [W					
Operation:	(Wns) →f					
Status Affected:	None					
Encoding:	1000	1fff	ffff	ffff	ffff	SSSS
Description:	register. Th	vord contents ne file register ut must be wc 'n.	may reside a	anywhere in t	he 32K word	s of data
		select the add select the so		-		
	Note 1: 2:	This instruction Since the file upper 15 bits assumed to b	register addr of the file reg	ess must be	word-aligned	
	3:	To move a by to f" instruc	te of data to f			10V WREG
Words:	1					
Cycles:	1					
Example 1: MO	V W4, XM	DOSRT ;	move W4 to	XMODSRT		
W/ XMODSR1 SF	Г 1340	XMODS	After Instructio W4 1200 RT 1200 SR 0000	n     		
Example 2: MO	∨ W8,0	x1222 ;	move W8 to	data addre	ss 0x1222	
W8 Data 1222 SF	2 FD88	Data 12	After Instructio W8 F200 222 F200 SR 0000	n ] -		

MOV.B		Move 8-bit I	_iteral to Wn	d		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MOV.B	#lit8,	Wnd		
Operands:	lit8 ∈ [0 Wnd ∈ [W					
Operation:	lit8 →Wnd					
Status Affected:	None					
Encoding:	1011	0011	1100	kkkk	kkkk	dddd
Description:		ned 8-bit literal of Wnd is not Ind.				
		specify the va select the ad This instructi	dress of the v	working regis		extension
		must be prov		jtoou		
Words:	1					
Cycles:	1					
Example 1:	MOV.B #0x1	7,W5;	load W5 wi	th #0x17 (B	yte mode)	
	Before Instruction W5 7899 SR 0000		After Instruction W5 7817 SR 0000	n   		
Example 2:	MOV.B #0×F	E,W9;	load W9 wi	th #0xFE (B	yte mode)	
	Before Instruction W9 AB23 SR 0000		After Instruction N9 ABFE SR 0000	n   		

#### 5

Instruction Descriptions

MOV		Move 16-bit	Literal to W	/nd		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MOV	#lit16,	Wnd		
Operands:	lit16 ∈ [-32 Wnd ∈ [W	768 65535 0 W15]	]			
Operation:	lit16 →Wno	t				
Status Affected:	None					
Encoding:	0010	kkkk	kkkk	kkkk	kkkk	dddd
Description:	The 16-bit be used fo	literal 'k' is loa r Wnd.	aded into Wn	d. Register d	irect address	sing must
		specify the v select the ad			ster.	
	2:	This instruction The literal ma or unsigned v	ay be specifie	ed as a signed		68:32767],
Words:	1	-	-	-		
Cycles:	1					
Example 1: MC	)V #0x4231	., W13 ;	load W13	with #0x423	1	
W1 SI			After Instructio 13 4231 SR 0000	n ] ]		
Example 2: MC	)V #0x4, ₩	12 ;	load W2 w	ith #0x4		
W			After Instructio V2 0004 SR 0000	-		
Example 3: MC	)V #-1000,	W8 ;	load W8 w	ith #-1000		
W			After Instructio V8 FC18 SR 0000	n ] ]		

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MOV{.B}	[Ws + Slit10],	Wnd		
Operands:		512 511] fo 024 1022]	r byte operatio (even only) fo		ation	
Operation:	[Ws + Slit1	0] →Wnd				
Status Affected:	None					
Encoding:	1001	0kkk	kBkk	kddd	dkkk	SSSS
	maintain w used for the The 'k' bits The 'B' bit The 'd' bits	ord address a e source, and specify the v selects byte o select the de	sed to [-1024 . alignment. Reg d direct addres value of the lite or word operati estination regis purce register.	gister indirect sing must be ral. ion ('0' for we	t addressing e used for W	must be 'nd.
		than a word i	n . B in the insi move. You may out it is not req	y use a .We		
		•				
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-me	odify-write ope	erations on no	, the listed cycl on-CPU Specia .1 "Multi-Cycl	al Function R	egisters. For	
Example 1: MC	OV.B [₩8+0	)x13], W10	; load W10	with [W8+0:	×13]	

Example 1:	MOV.	.B [W8	+0x13], W10	,	Load W10 (Byte mod	with [W8+0x13] de)
	I	Before nstructior	ı		After Instructior	ı
	W8	1008		W8	1008	
	W10	4009	١	W10	4033	

W8	1008	W8	1008
W10	4009	W10	4033
Data 101A	3312	Data 101A	3312
SR	0000	SR	0000

Example 2: MOV	7 [W4+0×	3E8], W2	; load W2 w ; (Word mod	ith [W4+0x3 e)	E8]	
W2 W4 Data 0BE8 SR	Before Instruction 9088 0800 5634 0000	Data 0B	After Instructio W2 5634 W4 0800 E8 5634 SR 0000	n       		
MOV		Move Wns	to [Wd with	offset]		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MOV{.B}	Wns,	[Wd + Slit10]		
Operands:	Slit10 ∈ [-5 Slit10 ∈ [-1	Wns ∈ [W0 W15] Slit10 ∈ [-512 511] in Byte mode Slit10 ∈ [-1024 1022] (even only) in Word mode Wd ∈ [W0 W15]				
Operation:	(Wns) →[W	/d + Slit10]				
Status Affected:	None					
Encoding:	1001	1kkk	kBkk	kddd	dkkk	SSSS
Description:	of Slit10 is maintain w	The contents of Wns are stored to [Wd + Slit10]. In Word mode, the range of Slit10 is increased to [-1024 1022] and Slit10 must be even to maintain word address alignment. Register direct addressing must be used for Wns, and indirect addressing must be used for the destination.				
	The 'B' bit s The 'd' bits	The 'k' bits specify the value of the literal. The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'd' bits select the destination register. The 's' bits select the source register.				
	1	than a word r word move, b	nove. You m out it is not re	•	xtension to c	lenote a
	<ol> <li>In Byte mode, the range of Slit10 is not reduced as specified in Section 4.6 "Using 10-bit Literal Operands", since the literat represents an address offset from Wd.</li> </ol>					
Words:	1					
Cycles:	1					
Example 1: MOV	″.B ₩0, [W		; store WO ; (Byte mod	to [W1+0x7] e)		
W0 W1 Data 1806 SR	Before Instruction 9015 1800 2345 0000	Data 18	After Instructio W0 9015 W1 1800 806 1545 SR 0000	n ] - -		

Example 2: MOV	W11, [W1		store W11 (Word mode	to [W1-0x4 e)	.00]	
ا W1 W11 Data 0C00 SR	Before Instruction 1000 8813 FFEA 0000	W: Data 0C0				
MOV		Move Ws to	Wd			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MOV{.B}	Ws, [Ws], [Ws++], [Ws], [Ws], [++Ws], [Ws + Wb],	Wd [Wd] [Wd++] [Wd] [Wd] [++Wd] [Wd + Wb]		
Operands:	Wb ∈ [W0.	Ws ∈ [W0 W15] Wb ∈ [W0 W15] Wd ∈ [W0 W15]				
Operation:	(Ws) →Wd					
Status Affected:	None					
Encoding:	0111	1www	wBhh	hddd	dggg	SSSS
Description:		ontents of the ster direct or in				
	The 'w' bits define the offset register Wb. The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'h' bits select the destination Address mode. The 'd' bits select the destination register. The 'g' bits select the source Address mode. The 's' bits select the source register.					
	<b>Note 1:</b> The extension . B in the instruction denotes a byte move rather than a word move. You may use a .W extension to denote a word move, but it is not required.					
	5					
	3: The instruction "PUSH Ws" translates to MOV Ws, [W15++].				W15++].	
	4:	The instructio	n "POP Wd" '	translates to	MOV [W1	5], Wd.

# **16-bit MCU and DSC Programmer's Reference Manual**

MOV			Move Ws to W	/d			
Words:		1					
Cycles:		1 <sup>(1)</sup>					
Note 1:	read-mod	ify-write op	erations on non-C	e listed cycle count does not apply to read an CPU Special Function Registers. For more 'Multi-Cycle Instructions".			
Example :	<u>1:</u> MOV	.B [W0-		e [W0] to W4 (Byte mode) -decrement W0			
		Before		After			
	I	nstruction		Instruction			
	W0	0A01	W0	0A00			
	W4	2976	W4	2989			
0	Data 0A00	8988	Data 0A00	8988			
	SR	0000	SR	0000			
Example :	<u>2:</u> MOV	[W6++],		love [W6] to [W2+W3] (Word mode) ost-increment W6			
		Before		After			
	1	nstruction		Instruction			
	W2	0800	W2	0800			
	W3	0040	W3	0040			
	W6	1228	W6	122A			
[	Data 0840	9870	Data 0840	0690			
[	Data 1228	0690	Data 1228	0690			
	SR	0000	SR	0000			
Ws ∈ [WC Wnd ∈ [M For direct Wns → Wns + : For indirect	/0, W2, W4 addressing of	W14] source:	Wnd	X	X		
---	---	---	---	---	--	--	--
Wns ∈ [W Ws ∈ [W0 Wnd ∈ [W For direct Wns → Wns + For indirect	/0, W2, W4 ) W15] /0, W2, W4 addressing of Wnd 1 →Wnd + 1	[Ws], [Ws++], [Ws], [++Ws], [Ws], W14] W14] source:	Wnd				
Ws ∈ [WC Wnd ∈ [M For direct Wns → Wns + : For indirect	) W15] /0, W2, W4 <sup>•</sup> addressing of Wnd 1 →Wnd + 1	[Ws++], [Ws], [++Ws], [Ws], W14] W14] source:					
Ws ∈ [WC Wnd ∈ [M For direct Wns → Wns + : For indirect	) W15] /0, W2, W4 <sup>•</sup> addressing of Wnd 1 →Wnd + 1	[Ws], [++Ws], [Ws], W14] W14] source:					
Ws ∈ [WC Wnd ∈ [M For direct Wns → Wns + : For indirect	) W15] /0, W2, W4 <sup>•</sup> addressing of Wnd 1 →Wnd + 1	[++Ws], [Ws], W14] W14] source:					
Ws ∈ [WC Wnd ∈ [M For direct Wns → Wns + : For indirect	) W15] /0, W2, W4 <sup>•</sup> addressing of Wnd 1 →Wnd + 1	[Ws], W14] W14] source:					
Ws ∈ [WC Wnd ∈ [M For direct Wns → Wns + : For indirect	) W15] /0, W2, W4 <sup>•</sup> addressing of Wnd 1 →Wnd + 1	W14] W14] source:					
Ws ∈ [WC Wnd ∈ [M For direct Wns → Wns + : For indirect	) W15] /0, W2, W4 <sup>•</sup> addressing of Wnd 1 →Wnd + 1	W14] source:					
Wns → Wns + : For indire	Wnd 1 →Wnd + 1						
Jee De	scription	of source:					
: None							
1011	1110	0000	0ddd	0ррр	SSSS		
Cription: Move the double word specified by the source to a destination worki register pair (Wnd:Wnd + 1). If register direct addressing is used for source, the contents of two successive working registers (Wns:Wns are moved to Wnd:Wnd + 1. If indirect addressing is used for the so Ws specifies the effective address for the least significant word of th double word. Any pre/post-increment or pre/post-decrement will adju by 4 bytes to accommodate for the double word.					d for the Wns + 1) e source, of the		
The 'p' bit	The 'd' bits select the destination register. The 'p' bits select the source Address mode. The 's' bits select the address of the first source register.						
Note 1:	<b>Note 1:</b> This instruction only operates on double words. See Figure for information on how double words are aligned in memory						
2: 3:				to MOV.D [	W15],		
1							
2(1)							
	None 1011 Move the register pa source, th are moved Ws specif double wo by 4 bytes The 'd' bit The 'p' bit The 's' bit Note 1: 2: 3: 1 2(1) sPIC33E and P d-modify-write of	None <u>1011</u> <u>1110</u> Move the double word s register pair (Wnd:Wnd source, the contents of t are moved to Wnd:Wnd Ws specifies the effectiv double word. Any pre/po by 4 bytes to accommod The 'd' bits select the de The 'p' bits select the de The 'p' bits select the ad <b>Note 1:</b> This instruction for information <b>2:</b> Wnd must be <b>3:</b> The instruction Wnd. 1 2 <sup>(1)</sup> sPIC33E and PIC24E devices d-modify-write operations on n	None         1011       1110       0000         Move the double word specified by the register pair (Wnd:Wnd + 1). If register source, the contents of two successivare moved to Wnd:Wnd + 1. If indired Ws specifies the effective address for double word. Any pre/post-increment by 4 bytes to accommodate for the dot The 'd' bits select the destination registre 'p' bits select the source Address of the 'd' bits select the address of the for information on how dout 2: Wnd must be an even wor 3: The instruction "POP.D Wn Wnd.         1       2(1)         sPIC33E and PIC24E devices, the listed cydemodify-write operations on non-CPU Spece	None         1011       1110       0000       0ddd         Move the double word specified by the source to a register pair (Wnd:Wnd + 1). If register direct addres source, the contents of two successive working reg are moved to Wnd:Wnd + 1. If indirect addressing Ws specifies the effective address for the least sign double word. Any pre/post-increment or pre/post-dby 4 bytes to accommodate for the double word.         The 'd' bits select the destination register.       The 'p' bits select the address of the first source re         Note 1:       This instruction only operates on double for information on how double words are 2:         Wnd must be an even working register.         3:       The instruction "POP.D Wnd" translates wnd.         1         2(1)         sPIC33E and PIC24E devices, the listed cycle count doe d-modify-write operations on non-CPU Special Function F	None         1011       1110       0000       0ddd       0ppp         Move the double word specified by the source to a destination v register pair (Wnd:Wnd + 1). If register direct addressing is used source, the contents of two successive working registers (Wns:V are moved to Wnd:Wnd + 1. If indirect addressing is used for th Ws specifies the effective address for the least significant word double word. Any pre/post-increment or pre/post-decrement will by 4 bytes to accommodate for the double word.         The 'd' bits select the destination register.         The 'bits select the address of the first source register.         Note 1:       This instruction only operates on double words. See for information on how double words are aligned in m         2:       Wnd must be an even working register.         3:       The instruction "POP.D Wnd" translates to MOV.D [wnd.         1		

5

MOV.D W2, W6

Example 1:

I W2 W3 W6 W7 SR <u>Example 2:</u> M0V	Before nstruction 12FB 9877 9833 FCC6 0000	W2 W3 W6 W7 SR ], W4 ; Move [	After Instruction 12FB 9877 12FB 9877 0000	V4 (Double mode)
I	Before nstruction		After	
W4	B012	W4	A319	
W5	FD89	W5	9927	
W7	0900	W7	08FC	
Data 0900	A319	Data 0900	A319	
Data 0902	9927	Data 0902	9927	
SR	0000	SR	0000	

; Move W2 to W6 (Double mode)

MOVPAG		Move Literal to Page Register				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	MOVPAG	#lit10,	DSRPAG		
	labolij		#lit9,	DSWPAG		
			#lit8,	TBLPAG		
Operands:	lit10 ∈ [0 .	1023], lit9 ∈	⊧ [0 511], li	it8 ∈ [0 25	5]	
Operation:	lit10 →DS	RPAG or lit9	→DSWPAG (	or lit8 $\rightarrow$ TBLF	PAG	
Status Affected:	None					
Encoding:	1111	1110	1100	PPkk	kkkk	kkkk
Description:	into the DS restricts th	priate numbe SRPAG, DSW e literal to a 9 and an 8-bit	/PAG, or TBL )-bit unsigned	PAG register d value when	. The assem the destinat	bler ion is
	The 'P' bits select the destination register. The 'k' bits specify the value of the literal.					
	Note:	This instruct	ion operates	in word mod	e only.	
Words:	1					
Cycles:	1					
Example 1: MOV	PAG #0x02,	DSRPAG				
	Before		After			
	Instruction		Instruction	ו		
DSRPAG	0000	DSRPA	AG 0002			

MOVPAG		Move Ws to	Page Regis	ster		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	MOVPAG	Wn,	DSRPAG		
				DSWPAG		
				TBLPAG		
Operands:	Wn∈ [W0	W15]				
Operation:	Wn<9:0> -	→DSRPAG or	Wn<8:0> →	DSWPAG or	Wn<7:0> $\rightarrow$	TBLPAG
Status Affected:	None					
Encoding:	1111	1110	1101	PP00	0000	SSSS
Description:	The appropriate number of bits from the register Ws are loaded into the DSRPAG, DSWPAG, or TBLPAG register. The assembler restricts the literal to a 9-bit unsigned value when the destination is DSWPAG, and 8-bit unsigned value when the destination is TBLPAG.					icts the
		select the de specify the s				
	Note:	This instruct	on operates	in word mod	e only.	
Words:	1					
Cycles:	1					
Example 1: MOVI	PAG W2, DSI	RPAG				
DSRPAG W2	Before Instruction 0000 0002	DSRPA V	After Instructior G 0002 /2 0002	1		

MOVSAC	Prefetch Operands and Store Accumulator						
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
				Х	Х	Х	
Syntax: {label:}	MOVSAC A	MOVSAC Acc {,[Wx], Wxd}			}	{,AWB}	
	$\{,[Wx] + = kx, Wxd\}$			$\{,[Wy] + = ky, Wyd\}$			
		{,[Wx] - = k	x, Wxd}	$\{,[Wy] - = ky, Wyd\}$			
		{,[W9 + W12	2], Wxd}	{,[W11 + W1	.2], Wyd}		
Operands:	Wy ∈ [W10,	W9]; kx ∈ [-6	[-6, -4, -2, 2,	, 6]; Wxd ∈  [' 4, 6]; Wyd ∈		I	
Operation:	([Wy]) →Wy	([Wx]) $\rightarrow$ Wxd; (Wx) + kx $\rightarrow$ Wx ([Wy]) $\rightarrow$ Wyd; (Wy) + ky $\rightarrow$ Wy (Acc(B or A)) rounded $\rightarrow$ AWB					
Status Affected:	None						
Encoding:	1100	0111	A0xx	yyii	iijj	jjaa	
Description:	instruction a though an a	and optionally ccumulator o	/ store the un operation is r	aration for ar nspecified ac not performe signate whicl	cumulator re d in this instr	esults. Ever uction, an	
	Operands Wx, Wxd, Wy and Wyd specify optional prefetch operations which support indirect and register offset addressing, as described in Section 4.14.1 "MAC Prefetches". Operand AWB specifies the optional store of the "other" accumulator, as described in Section 4.14.4 "MAC Write Back".						
The 'A' bit selects the other accumulator used for write back. The 'x' bits select the prefetch Wxd destination. The 'y' bits select the prefetch Wyd destination. The 'i' bits select the Wx prefetch operation. The 'j' bits select the Wy prefetch operation. The 'a' bits select the accumulator Write Back destination.							
Words:	1						
Cycles:	1						

```
Example 1:
```

MOVSAC B, [W9], W6, [W11]+=4, W7, W13 ; Fetch [W9] to W6

; Fetch [W11] to W7, Post-increment W11 by 4

; Store ACCA to W13

	Before Instruction		After Instruction
W6	A022	W6	7811
W7	B200	W7	B2AF
W9	0800	W9	0800
W11	1900	W11	1904
W13	0020	W13	3290
ACCA	00 3290 5968	ACCA	00 3290 5968
Data 0800	7811	Data 0800	7811
Data 1900	B2AF	Data 1900	B2AF
SR	0000	SR	0000

Example 2: MOVSAC A, [W9]-=2, W4, [W11+W12], W6, [W13]+=2 ; Fetch [W9] to W4, Post-decrement W9 by 2

; Fetch [W11+W12] to W6

; Store ACCB to [W13], Post-increment W13 by 2

	Before Instruction
W4	76AE
W6	2000
W9	1200
W11	2000
W12	0024
W13	2300
ACCB	00 9834 4500
Data 1200	BB00
Data 2024	52CE
Data 2300	23FF
SR	0000

	After Instruction
W4	BB00
W6	52CE
W9	11FE
W11	2000
W12	0024
W13	2302
ACCB	00 9834 4500
Data 1200	BB00
Data 2024	52CE
Data 2300	9834
SR	0000

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
				X	X	X		
Syntax: {label:}	MPY Wm	MPY Wm * Wn, Acc {,[Wx], Wxd} {,[Wx] + = kx, Wxd}				{,[Wy], Wyd} {,[Wy] + = ky, Wyd}		
			{,[Wx] – = k	-	$\{,[Wy] - = k$			
			{,[W9 + W12	-	{,[W11 + W1			
Operands: Operation:	Acc $\in$ [A,B] Wx $\in$ [W8, Wy $\in$ [W10 AWB $\in$ [W10 (Wm) * (Wm ([Wx]) $\rightarrow$ W2	- W9]; kx ∈ [-	<sup>-</sup> B) < →Wx	, 6]; Wxd ∈ [	W4 W7]			
Status Affected:		AB, SA, SB,	-					
Encoding:	1100	Ommm	A0xx	yyii	iijj	jj11		
Description:	operands in	preparation d multiply is	two working for another M sign-extende	1AC type inst	ruction. The	32-bit resul		
	Operands Wx, Wxd, Wy and Wyd specify optional prefetch operations which support indirect and register offset addressing, as described in <b>Section 4.14.1 "MAC Prefetches</b> ".							
	elects the a select the pr select the pr select the W select the W fhe IF bit, C ractional or		or the result. destination. destination. eration. eration. determines	if the multiply	<i>i</i> s			
	2:	۲he US<1:0	> bits (CORC					
	( r		2> in dsPIC3 Isigned, signe Port mixed-sig	ed, or mixed	sign. Only d			
Words:	( r	nultiply is ur	signed, signe	ed, or mixed	sign. Only d			

```
Example 1:
```

MPY W4\*W5, A, [W8]+=2, W6, [W10]-=2, W7

- ; Multiply W4\*W5 and store to ACCA
- ; Fetch [W8] to W6, Post-increment W8 by 2  $\,$
- ; Fetch [W10] to W7, Post-decrement W10 by 2
- ; CORCON = 0x0000 (fractional multiply, no saturation)

	Before Instruction		After Instruction
W4	C000	W4	C000
W5	9000	W5	9000
W6	0800	W6	671F
W7	B200	W7	E3DC
W8	1780	W8	1782
W10	2400	W10	23FE
ACCA	FF F780 2087	ACCA	00 3800 0000
Data 1780	671F	Data 1780	671F
Data 2400	E3DC	Data 2400	E3DC
CORCON	0000	CORCON	0000
SR	0000	SR	0000

Example 2:

- MPY W6\*W7, B, [W8]+=2, W4, [W10]-=2, W5
- ; Multiply W6\*W7 and store to ACCB ; Fetch [W8] to W4, Post-increment W8 by 2
- ; Fetch [W10] to W5, Post-decrement W10 by 2
- ; CORCON = 0x0000 (fractional multiply, no saturation)
- CORCON 0x0000 (Tractional multiply, no saturation)

	Before		After
	Instruction		Instruction
W4	C000	W4	8FDC
W5	9000	W5	0078
W6	671F	W6	671F
W7	E3DC	W7	E3DC
W8	1782	W8	1784
W10	23FE	W10	23FC
ACCB	00 9834 4500	ACCB	FF E954 3748
Data 1782	8FDC	Data 1782	8FDC
Data 23FE	0078	Data 23FE	0078
CORCON	0000	CORCON	0000
SR	0000	SR	0000

MPY		Square to I	Accumulato	r		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
				Х	Х	Х
Syntax: {label:}	MPY Wm *	Wm, Acc	{,[Wx], Wxd	}	{,[Wy], Wyd	}
			{,[Wx] + = kx	k, Wxd}	{,[Wy] + = k	y, Wyd}
			{,[Wx] - = k	x, Wxd}	{,[Wy] – = ky	y, Wyd}
			{,[W9 + W12	2], Wxd}	{,[W11 + W1	.2], Wyd}
Operands:	$\begin{array}{l} ACC \in \ [A,B] \\ WX \in \ [W8, \end{array} \end{array}$	_ W9]; kx ∈ [-6	W5 * W5, W 6, -4, -2, 2, 4 [-6, -4, -2, 2,	, 6]; Wxd ∈ [	-	
Operation:	([Wx]) →W>	(Wm) * (Wm) →Acc(A or B) ([Wx]) →Wxd; (Wx) + kx →Wx ([Wy]) →Wyd; (Wy) + ky →Wy				
Status Affected:	OA, OB, OA	AB, SA, SB, S	SAB			
Encoding:	1111	00mm	A0xx	yyii	iijj	jj01
Description:	Square the contents of a working register, optionally prefetch operands in preparation for another MAC type instruction. The 32-bit result of the signed multiply is sign-extended to 40 bits and stored in the specified accumulator.					
	Operands Wx, Wxd, Wy and Wyd specify optional prefetch operations which support indirect and register offset addressing, as described in <b>Section 4.14.1 "MAC Prefetches"</b> .					
	The 'A' bit s The 'x' bits The 'y' bits The 'i' bits s The 'j' bits s Note 1:	elects the ac select the pr select the pr select the Wy select the Wy The IF bit (Co ractional or a The US<1:0>	an integer. • bits (CORC	r the result. lestination. lestination. eration. , determines ON<13:12>	if the multipl	,
	(   	CORCON<12 multiply is un	2> in dsPIC3	0F/dsPIC33I ed, or mixed-	F) determine ·sign. Only d	if the
Words:	1					
Cycles:	1					

Example 1:

MPY W6\*W6, A, [W9]+=2, W6

- ; Square W6 and store to ACCA
- ; Fetch [W9] to W6, Post-increment W9 by 2  $\ensuremath{\mathsf{2}}$
- ; CORCON = 0x0000 (fractional multiply, no saturation)

	Before Instruction		After Instruction
W6	6500	W6	B865
W9	0900	W9	0902
ACCA	00 7C80 0908	ACCA	00 4FB2 0000
Data 0900	B865	Data 0900	B865
CORCON	0000	CORCON	0000
SR	0000	SR	0000

Example 2: MPY W4\*W4, B, [W9+W12], W4, [W10]+=2, W5

- ; Square W4 and store to ACCB
- ; Fetch [W9+W12] to W4
- ; Fetch [W10] to W5, Post-increment W10 by 2
- ; CORCON = 0x0000 (fractional multiply, no saturation)

	Before Instruction			
W4	E228			
W5	9000			
W9	1700			
W10	1B00			
W12	FF00			
ACCB	00 9834 4500			
Data 1600	8911			
Data 1B00	F678			
CORCON	0000			
SR	0000			

	After Instruction
W4	8911
W5	F678
W9	1700
W10	1B02
W12	FF00
ACCB	00 06F5 4C80
Data 1600	8911
Data 1B00	F678
CORCON	0000
SR	0000

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
implemented in.	110241	1102411	11024	X	X	X
Syntax: {label:}	MPY.N Wm * Wn, Acc		{,[Wx], Wxd {,[Wx] + = k>	k, Wxd}	{,[Wy], Wyd} {,[Wy] + = ky, Wyd} {,[Wy] – = ky, Wyd}	
			$\{,[Wx] - = kx \}$ $\{,[W9 + W12]$		{,[Wy] – = ky {,[W11 + W1	
Operands:	$Acc \in [A,B]$ $Wx \in [W8, Y]$	- W9]; kx ∈ [-6	6, -4, -2, 2, 4	, 6]; Wxd ∈ [	W6; W5 * W W4 W7] ₌ [W4 W7]	
Operation:	([Wx]) →Wx	n) →Acc(A o d; (Wx) + kx rd; (Wy) + ky	→Wx			
Status Affected:	OA, OB, OA	B				
Encoding:	1100	Ommm	A1xx	yyii	iijj	jj11
Description:	Multiply the of another w				negative of t erands in pre	
	accumulato	C type instruct r results. The	ction and opt e 32-bit resul	ionally store t of the signe	the unspecified multiply is ed accumula	ied
	accumulato sign-extend The 'm' bits The 'A' bit s The 'y' bits s The 'j' bits s The 'j' bits s Note 1:	C type instruct r results. The ed to 40 bits select the op elects the ac select the pro- select the pro- elect the Wy elect the Wy The IF bit (CC	ction and opt e 32-bit resul and stored t perand regis ccumulator fo efetch Wxd c efetch Wyd c c prefetch op prefetch op DRCON<0>)	ionally store t of the signe to the specifi ters Wm and or the result. Jestination. Jestination. eration. eration.	the unspecifed multiply is	ied tor. nultiply.
	accumulato sign-extend The 'm' bits The 'A' bits s The 'y' bits s The 'j' bits s Note 1: T fi 2: T	C type instruct r results. The ed to 40 bits select the op elects the ac select the pro- select the the elect the Wy che IF bit (CC ractional or a che US<1:0> CORCON<12 nultiply is un	ction and opt e 32-bit resul and stored t perand regist ccumulator for efetch Wxd c efetch Wyd c prefetch op prefetch op DRCON<0>) an integer. bits (CORC 2> in dsPIC3	ionally store t of the signe to the specifi ters Wm and or the result. destination. eration. eration. , determines ON<13:12> OF/dsPIC331 ed, or mixed	the unspecif ed multiply is ed accumula Wn for the r if the multipl in dsPIC33E -) determine sign. Only ds	ied tor. nultiply. ly is , if the
Words:	accumulato sign-extend The 'm' bits The 'A' bits s The 'y' bits s The 'j' bits s Note 1: T fi 2: T	C type instruct r results. The ed to 40 bits select the op elects the ac select the pro- select the the elect the Wy che IF bit (CC ractional or a che US<1:0> CORCON<12 nultiply is un	ction and opt e 32-bit resul and stored t perand regist ccumulator for efetch Wxd c efetch Wyd c prefetch op prefetch op DRCON<0>) an integer. bits (CORC 2> in dsPIC3 signed, signed	ionally store t of the signe to the specifi ters Wm and or the result. destination. eration. eration. , determines ON<13:12> OF/dsPIC331 ed, or mixed	the unspecif ed multiply is ed accumula Wn for the r if the multipl in dsPIC33E -) determine sign. Only ds	ied tor. nultiply. ly is , if the

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Instruction Descriptions

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Example 1:
```

MPY.N W4\*W5, A, [W8]+=2, W4, [W10]+=2, W5 ; Multiply W4\*W5, negate the result and store to ACCA ; Fetch [W8] to W4, Post-increment W8 by 2

- ; Fetch [W10] to W5, Post-increment W10 by 2
- ; CORCON = 0x0001 (integer multiply, no saturation)

	Before Instruction		After Instruction
W4	3023	W4	0054
W5	1290	W5	660A
W8	0B00	W8	0B02
W10	2000	W10	2002
ACCA	00 0000 2387	ACCA	FF FC82 7650
Data 0B00	0054	Data 0B00	0054
Data 2000	660A	Data 2000	660A
CORCON	0001	CORCON	0001
SR	0000	SR	0000

Example 2:

MPY.N W4\*W5, A, [W8]+=2, W4, [W10]+=2, W5 ; Multiply W4\*W5, negate the result and store to ACCA

; Fetch [W8] to W4, Post-increment W8 by 2

; Fetch [W10] to W5, Post-increment W10 by 2

; CORCON = 0x0000 (fractional multiply, no saturation)

	Before Instruction		After Instruction
W4	3023	W4	0054
W5	1290	W5	660A
W8	0B00	W8	0B02
W10	2000	W10	2002
ACCA	00 0000 2387	ACCA	FF F904 ECA0
Data 0B00	0054	Data 0B00	0054
Data 2000	660A	Data 2000	660A
CORCON	0000	CORCON	0000
SR	0000	SR	0000

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
				Х	Х	Х	
Syntax: {label:}	MSC Wm	* Wn, Acc	{,[Wx], Wxd	}	{,[Wy], Wyd	} {,AWB	
			{,[Wx] + = kx	k, Wxd}	{,[Wy] + = k	y, Wyd}	
			{,[Wx] − = k	x, Wxd}	{,[Wy] – = ky	y, Wyd}	
			{,[W9 + W12	2], Wxd}	{,[W11 + W1	.2], Wyd}	
Operands:	$\begin{array}{l} Acc \in \ [A,B] \\ Wx \in \ [W8, \\ Wy \in \ [W10] \end{array}$	] W9]; kx ∈ [-	W4 * W6, W4 6, -4, -2, 2, 4 [-6, -4, -2, 2, = 2]	, 6]; Wxd ∈ [	W4 W7]		
Operation:	([Wx]) →Wx ([Wy]) →Wy	8)) –(Wm) * (' kd; (Wx) + kx yd; (Wy) + ky s)) rounded –	/ →Wy	or B)			
Status Affected:	OA, OB, OA	AB, SA, SB,	SAB				
Encoding:	1100	Ommm	A1xx	yyii	iijj	jjaa	
Description:	operands in store the ur	n preparation nspecified ac sign-extende	two working i for another l ccumulator re d to 40 bits a	MAC type ins sults. The 32	truction and o 2-bit result of	optionally the signed	
	Operands Wx, Wxd, Wy and Wyd specify optional prefetch operations which support indirect and register offset addressing as described in <b>Section 4.14.1 "MAC Prefetches"</b> . Operand AWB specifies the optional store of the "other" accumulator as described in <b>Section 4.14.4 "MAC Write Back</b> ".						
	Section 4.1 store of the	L4.1 "MAC F "other" accu	nd register o Prefetches". Imulator as d	Operand AV		ibed in	
	Section 4.1 store of the Section 4.1 The 'm' bits The 'A' bits The 'A' bits The 'y' bits The 'j' bits The 'j' bits	<b>14.1 "MAC F</b> "other" accu <b>14.4 "MAC V</b> selects the or select the pr select the pr select the pr select the Wi select the Wi	nd register o Prefetches". Imulator as d	Operand AW escribed in ters Wm and r the result. lestination. lestination. eration. eration.	/B specifies t	ibed in the optiona	
	Section 4.1 store of the Section 4.1 The 'm' bits The 'A' bits The 'A' bits The 'y' bits The 'j' bits The 'j' bits The 'a' bits Note:	<b>14.1 "MAC F</b> "other" accu <b>14.4 "MAC V</b> selects the of selects the ac select the pr select the pr select the Wa select the Wa select the Wa	and register o Prefetches". Imulator as d Vrite Back". perand regis ccumulator for efetch Wxd o efetch Wyd o x prefetch op y prefetch op ccumulator W CORCON<0>	Operand AW escribed in ters Wm and or the result. lestination. lestination. eration. rite Back de	/B specifies t I Wn for the r stination.	ibed in the optiona nultiply.	
Words:	Section 4.1 store of the Section 4.1 The 'm' bits The 'A' bits The 'A' bits The 'y' bits The 'j' bits The 'j' bits The 'a' bits Note:	L4.1 "MAC F "other" accu L4.4 "MAC V s select the of selects the ac select the pr select the pr select the W select the W select the W select the ac The IF bit (C	and register o Prefetches". Imulator as d Vrite Back". perand regis ccumulator for efetch Wxd o efetch Wyd o x prefetch op y prefetch op ccumulator W CORCON<0>	Operand AW escribed in ters Wm and or the result. lestination. lestination. eration. rite Back de	/B specifies t I Wn for the r stination.	ibed in the optiona nultiply.	

```
Example 1:
```

MSC W6\*W7, A, [W8]-=4, W6, [W10]-=4, W7 ; Multiply W6\*W7 and subtract the result from ACCA ; Fetch [W8] to W6, Post-decrement W8 by 4 ; Fetch [W10] to W7, Post-decrement W10 by 4

; CORCON = 0x0001 (integer multiply, no saturation)

	Before Instruction		After Instruction
W6	9051	W6	D309
W7	7230	W7	100B
W8	0C00	W8	0BFC
W10	1C00	W10	1BFC
ACCA	00 0567 8000	ACCA	00 3738 5ED0
Data 0C00	D309	Data 0C00	D309
Data 1C00	100B	Data 1C00	100B
CORCON	0001	CORCON	0001
SR	0000	SR	0000

Example 2:

<u>2:</u> MSC W4\*W5, B, [W11+W12], W5, W13

; Multiply W4\*W5 and subtract the result from ACCB

; Fetch [W11+W12] to W5

; Write Back ACCA to W13

; CORCON = 0x0000 (fractional multiply, no saturation)

	Before
	Instruction
W4	0500
W5	2000
W11	1800
W12	0800
W13	6233
ACCA	00 3738 5ED0
ACCB	00 1000 0000
Data 2000	3579
CORCON	0000
SR	0000

	After Instruction
W4	0500
W5	3579
W11	1800
W12	0800
W13	3738
ACCA	00 3738 5ED0
ACCB	00 0EC0 0000
Data 2000	3579
CORCON	0000
SR	0000

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MUL{.B}	f			
Operands:	f∈ [0 81	191]				
Operation:	For word o	)<7:0> * (f)<7				
Status Affected:	None					
Encoding:	1011	1100	0B0f	ffff	ffff	ffff
Description:		e default work				
Description:	register an and the res executed in the most s	e default work d place the re- sult are interp n Byte mode, ignificant word icant word of	esult in the V reted as uns the 16-bit re d of the 32-b	V2:W3 regist signed intege esult is stored bit result is st	er pair. Both rs. If this ins I in W2. In W ored in W3, a	operands truction is /ord mode,
Description:	register an and the res executed in the most s least signif The 'B' bit	d place the re sult are interp n Byte mode, ignificant wor	esult in the V reted as uns the 16-bit re d of the 32-b the 32-bit re or word oper	V2:W3 regist signed intege esult is stored bit result is st esult is stored ation ('0' for	er pair. Both rs. If this ins I in W2. In W ored in W3, a I in W2.	operands truction is /ord mode, and the
Description:	register an and the res executed in the most s least signif The 'B' bit The 'f' bits Note 1:	d place the re sult are interp n Byte mode, ignificant word icant word of selects byte o	esult in the V reted as uns the 16-bit re d of the 32-b the 32-bit re or word oper dress of the n . B in the i word operat	V2:W3 regist signed intege esult is stored bit result is st esult is stored ation ('0' for file register. Instruction de tion. You may	er pair. Both rs. If this ins I in W2. In W ored in W3, a I in W2. word, '1' for notes a byte y use a . W es	operands truction is /ord mode, and the byte). operation
Description:	register an and the re- executed in the most s least signif The 'B' bit The 'f' bits <b>Note 1:</b>	d place the re- sult are interp in Byte mode, ignificant word icant word of selects byte of select the ad The extensio rather than a	esult in the V reted as uns the 16-bit re d of the 32-b the 32-bit re or word oper dress of the n . B in the i word operation,	V2:W3 regist signed intege sult is stored it result is st sult is stored ation ('0' for file register. nstruction de tion. You may but it is not i	er pair. Both rs. If this ins I in W2. In W ored in W3, a I in W2. word, '1' for notes a byte y use a .W e required.	operands truction is /ord mode, and the byte). operation
Description:	register an and the res executed in the most s least signif The 'B' bit The 'f' bits Note 1: 2: 3:	d place the re- sult are interp in Byte mode, ignificant word icant word of selects byte of select the ad The extensio rather than a denote a wor The WREG is The IF bit (CO	esult in the V reted as uns the 16-bit re d of the 32-bit the 32-bit re or word oper dress of the n . B in the i word operation, s set to work ORCON<0>	V2:W3 regist signed intege esult is stored bit result is stored ation ('0' for file register. Instruction de tion. You may but it is not i king register ' ), has no effe	er pair. Both rs. If this ins I in W2. In W ored in W3, a I in W2. word, '1' for notes a byte y use a .W ez required. W0. ect on this op	operands truction is (ord mode, and the byte). operation ktension to eration.
Description:	register an and the res executed in the most s least signif The 'B' bit The 'f' bits <b>Note 1:</b> 2:	d place the re- sult are interp in Byte mode, ignificant word icant word of selects byte of select the ad The extensio rather than a denote a wor The WREG is	esult in the V reted as uns the 16-bit re d of the 32-bit the 32-bit re or word oper dress of the n . B in the i word operation, s set to work ORCON<0>	V2:W3 regist signed intege esult is stored bit result is stored ation ('0' for file register. Instruction de tion. You may but it is not i king register ' ), has no effe	er pair. Both rs. If this ins I in W2. In W ored in W3, a I in W2. word, '1' for notes a byte y use a .W ez required. W0. ect on this op	operands truction is (ord mode, and the byte). operation ktension to eration.
Description: Words:	register an and the res executed in the most s least signif The 'B' bit The 'f' bits Note 1: 2: 3:	d place the re- sult are interp in Byte mode, ignificant word icant word of selects byte of select the ad The extensio rather than a denote a wor The WREG is The IF bit (Co This is the or	esult in the V reted as uns the 16-bit re d of the 32-bit the 32-bit re or word oper dress of the n . B in the i word operation, s set to work ORCON<0>	V2:W3 regist signed intege esult is stored bit result is stored ation ('0' for file register. Instruction de tion. You may but it is not i king register ' ), has no effe	er pair. Both rs. If this ins I in W2. In W ored in W3, a I in W2. word, '1' for notes a byte y use a .W ez required. W0. ect on this op	operands truction is (ord mode, and the byte). operation ktension to eration.

#### Note 1: In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1: MUL	.B 0x800	; Multiply (	0×800)*WRE	G (Byte mode)
	Before Instruction		After Instruction	
WREG (W0)	9823	WREG (W0)	9823	
W2	FFFF	W2	13B0	
W3	FFFF	W3	FFFF	
Data 0800	2690	Data 0800	2690	
SR	0000	SR	0000	

Example 2: MUL	TMR1	; Multiply (	TMR1)*WREG	(Word mode)
I	Before nstruction		After Instruction	
WREG (W0)	F001	WREG (W0)	F001	
W2	0000	W2	C287	
W3	0000	W3	2F5E	
TMR1	3287	TMR1	3287	
SR	0000	SR	0000	

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MUL.SS	Wb,	Ws,	Wnd	
,	C J			[Ws],		
				[Ws++],		
				[Ws],		
				[++Ws],		
				[Ws],		
Operands:	Wb∈ [W0					
	$Ws \in [W0]$	W15] 0, W2, W4	14/1 21			
Operation:		b) * signed (V		Vnd + 1		
Status Affected:	None	b) Signed (v	vs) —vviiu.v			
Encoding:	1011	1001	1www	wddd	dnnn	6666
Description:		e contents of			dppp	SSSS
	the result i register), a	s stored in W and the most	significant w	ord of the res	en numbered sult is stored	d working in
	the result register), a Wnd + 1. I two's com used for W	s stored in W	nd (which m significant w perands and ed integers.	iust be an ev ord of the res d the result V Register dire	en numbered sult is stored /nd are inter ct addressing	d working in preted as g must be
	the result i register), a Wnd + 1. I two's com used for W may be us The 'w' bit The 'd' bits The 'p' bits	s stored in W and the most Both source c plement signe /b and Wnd.	and (which m significant w operands and ed integers. I Register dire ddress of the ddress of the burce Addres	ust be an ev ord of the res d the result V Register dire ect or register e base regist e lower destir ss mode.	en numbered sult is stored /nd are inter ct addressing indirect add er.	d working in preted as g must be ressing
	the result i register), a Wnd + 1. I two's com used for W may be us The 'w' bit The 'd' bits The 'p' bits	s stored in W and the most Both source of plement signe /b and Wnd. I red for Ws. s select the a s select the a s select the so	and (which m significant w perands and ed integers. I Register dire ddress of the ddress of the burce Addres	ust be an ev ord of the res d the result V Register dire ect or register e base regist e lower destir ss mode. er.	en numbered sult is stored Vnd are inter ct addressing indirect add er. nation registe	d working in preted as g must be ressing
	the result i register), a Wnd + 1. I two's com used for W may be us The 'w' bit The 'd' bits The 'p' bits	s stored in W and the most Both source of plement signe /b and Wnd. I ed for Ws. s select the a s select the a s select the so s select the so This instructi Since the pro an even wor	Ind (which m significant w operands and ed integers. I Register dire ddress of the ddress of the ddress of the ource Addres ource register on operates oduct of the r king register	ust be an ev ord of the res d the result V Register dire ect or register e base regist e lower destir ss mode. er. in Word moo nultiplication . See Figure	en numbered sult is stored Vnd are inter ct addressing indirect add er. nation registe de only. is 32 bits, Wi 4-2 for inform	d working in preted as g must be ressing er.
	the result i register), a Wnd + 1. I two's com used for W may be us The 'w' bit The 'd' bits The 'p' bits The 's' bits <b>Note 1:</b> 2:	s stored in W and the most Both source of plement signe /b and Wnd. I ded for Ws. s select the ad s select the ad s select the so s select the so This instruction Since the pro- an even work how double	and (which m significant w perands and ed integers. I Register dire ddress of the ddress of the burce Addres ource register on operates oduct of the r king register words are al	iust be an ev ord of the res d the result W Register dire ect or register e base regist e lower destir ss mode. er. in Word moo nultiplication . See Figure igned in men	en numbered sult is stored Vnd are inter ct addressing indirect add er. nation registe de only. is 32 bits, Wi 4-2 for inform nory.	d working in preted as g must be ressing er. er. nd must be nation on
	the result i register), a Wnd + 1. I two's com used for W may be us The 'w' bit The 'd' bits The 'f' bits The 's' bits <b>Note 1:</b>	s stored in W and the most a Both source of plement signed /b and Wnd. I ded for Ws. s select the ad s select the ad s select the so This instruction Since the pro- an even work how double of Wnd may no The IF bit an	and (which m significant w perands and ed integers. I Register dire ddress of the ddress of the burce Addres ource register on operates oduct of the r king register words are al t be W14, si d the US<1:(	ust be an ev ord of the res d the result V Register dire ect or register e base regist e lower destir ss mode. er. in Word mod nultiplication . See Figure igned in men nce W15<0> D> bits in the	en numbered sult is stored Vnd are inter ct addressing indirect add er. hation registe de only. is 32 bits, Wi 4-2 for inform hory. is fixed to ze	d working in preted as g must be ressing er. er. nd must be nation on ero.
Words:	the result i register), a Wnd + 1. I two's com used for W may be us The 'w' bit The 'd' bits The 'bits The 's' bits <b>Note 1:</b> 2: <b>3:</b>	s stored in W and the most a Both source of plement signe /b and Wnd. I ded for Ws. s select the ad s select the ad s select the so This instructi Since the pro- an even work how double w	and (which m significant w perands and ed integers. I Register dire ddress of the ddress of the burce Addres ource register on operates oduct of the r king register words are al t be W14, si d the US<1:(	ust be an ev ord of the res d the result V Register dire ect or register e base regist e lower destir ss mode. er. in Word mod nultiplication . See Figure igned in men nce W15<0> D> bits in the	en numbered sult is stored Vnd are inter ct addressing indirect add er. hation registe de only. is 32 bits, Wi 4-2 for inform hory. is fixed to ze	d working in preted as g must be ressing er. er. nd must be nation on ero.

details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

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Example 1:	MUL.SS W0, W1	, W12 ; Multiply W0*W1 ; Store the result to W12:W13
	Before Instruction W0 9823 W1 67DC W12 FFFF	After Instruction W0 9823 W1 67DC W12 D314
	W13 FFFF SR 0000	W13 D5DC SR 0000
Example 2:	MUL.SS W2, [-	-W4], W0 ; Pre-decrement W4 ; Multiply W2*[W4] ; Store the result to W0:W1
	Before Instruction W0 FFFF	After Instruction W0 28F8
	W1 FFFF W2 0045	W1 0000 W2 0045
Data	W4         27FE           27FC         0098           SR         0000	W4         27FC           Data 27FC         0098           SR         0000

MUL.SS		Destinatio	-			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
				<u> </u>		Х
Syntax:	{label:}	MUL.SS	Wb,	Ws,		
- ,	,			[Ws],	А	
				[Ws++],	В	
				[Ws],		
				[++Ws],		
				[Ws],		
Operands:	Wb ∈ [W0 Ws ∈ [W0 ACC ∈ [A,	) W15]				
Operation:	_	/b) * signed (\	Ws) →ACC(/	A or B)		
Status Affected:	None	-				
Encoding:	1011	1001	1www	w111	Аррр	SSSS
Description:	stored in o 32-bit resu target accu	one of the DS ult is sign exte umulator.	SP engine action of the second	nultiply with a ccumulators, A 39 prior to be	ACCA or ACC eing loaded in	CB. The nto the
	depending	g upon the op	perating mode	s integer or fr le of the DSP ource operanc	engine (as d	defined by
	The 'd' bits The 'p' bits	s select the a select sourc	address of the rce Address n	ne base regist le source regi mode 2. ccumulator fo	ister.	t.
				es in Word mo		
		The state o	of the multipli	lier mode bits e operation of	s (US<1:0> in	
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-moo details, s	C33E and PIC2 dify-write oper see <b>Note 3</b> in \$	erations on no Section 3.2.3	on-CPU Speci	ial Function F	Registers. For	
Example 1: MUL	L.SS W0, W1	Ι, Α				
	Before	e		After		
	Instructio	ion		Instruction	_	
W0	1	9823	W0	982	23	
\\/1		2200	14/1	670		
W1 Acc A		67DC 0000	W1 Acc A F	67D F D5DC D31		

Instruction Descriptions

MUL.SU	J	Integer 16x	16-bit Signe	ed-Unsigned	Short Liter	al Multiply
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MUL.SU	Wb,	#lit5,	Wnd	
Operands:	lit5 ∈ [0	/0 W15] 31] W0, W2, W4	W12]			
Operation:	signed (\	Wb) * unsigned	l lit5 →Wnd:\	Vnd + 1		
Status Affected:	None					
Encoding:	1011	1001	0www	wddd	d11k	kkkk
	the resul register). The Wb complem integer. F The 'w' b	result in two successive working registers. The least significant word of the result is stored in Wnd (which must be an even numbered working register), and the most significant word of the result is stored in Wnd + 1. The Wb operand and the result Wnd are interpreted as a two's complement signed integer. The literal is interpreted as an unsigned integer. Register direct addressing must be used for Wb and Wnd. The 'w' bits select the address of the base register. The 'd' bits select the address of the lower destination register.				
	Note 1: 2: 3: 4:	Since the pro an even wor how double	oduct of the r king register words are ali ot be W14, si d the US<1:0	nultiplication See Figure gned in mem nce W15<0> )> bits in the	is 32 bits, W 4-3 for inform nory. is fixed to ze	nation on ero.
Words:	1		·			
Cycles:	1					
Example 1:	MUL.SU WO,	#0x1F, W2 ; ;		0 by liter result to 1		
	Before Instruction W0 C000 W2 1234 W3 C9BA SR 0000	M M	After Instruction /0 C000 /2 4000 /3 FFF8 R 0000	I		

Example 2:	MUL.	SU W2,	#0x10,	WO	'		V2 by literal 0x10 result to W0:W1
		Before				After	
	Ir	nstructior	า	Instruction			า
	W0	ABCD			W0	2400	
	W1	89B3			W1	000F	
	W2	F240			W2	F240	
	SR	0000			SR	0000	

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
·	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	MUL.SU	Wb,	Ws,	Wnd			
				[Ws],				
				[Ws++],				
				[Ws],				
				[++Ws],				
				[Ws],				
Operands:	$Wb \in [WC]$ $Ws \in [WC]$ $Wnd \in [W]$		W12]					
Operation:	signed (W	b) * unsigned	(Ws) →Wno	l:Wnd + 1				
Status Affected:	None	-		1				
Encoding:	1011	1001	0www	wddd	dppp	SSSS		
Description:	result in tw the result register), a The Wb o compleme unsigned	Multiply the contents of Wb with the contents of Ws, and store the 32-bit result in two successive working registers. The least significant word of the result is stored in Wnd (which must be an even numbered working register), and the most significant word of the result is stored in Wnd + 1. The Wb operand and the result Wnd are interpreted as a two's complement signed integer. The Ws operand is interpreted as an unsigned integer. Register direct addressing must be used for Wb and Wnd. Register direct or register indirect addressing may be used for Ws.						
	The 'd' bit The 'p' bit	The 'w' bits select the address of the base register. The 'd' bits select the address of the lower destination register. The 'p' bits select the source Address mode. The 's' bits select the source register.						
	Note 1:	This instructi	on operates	in Word mod	le only.			
	2:	2: Since the product of the multiplication is 32 bits, Wnd must be an even working register. See Figure 4-3 for information on how double words are aligned in memory.						
	3:	Wnd may no	t be W14, si	nce W15<0>	is fixed to ze	ero.		
	4:	The IF bit an no effect on		0> bits in the n.	CORCON re	gister have		
Words:	1							
Cycles:	1(1)							

details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1:	MUL.SU W8, [	wal, wo ; mulliply war[wa]
		; Store the result to WO:W1
	Before	After
	Instruction	Instruction
	W0 68DC	W0 0000
	W1 AA40	W1 F100
	W8 F000	W8 F000
	W9 178C	W9 178C
Data 1		Data 178C F000
	SR 0000	SR 0000
Example 2:	MUL.SU W2, [	[++W3], W4 ; Pre-Increment W3
		; Multiply W2*[W3] ; Store the result to W4:W5
	Before	After
	Instruction	Instruction
	W2 0040	W2 0040
	W3 0280	W3 0282
	W4 1819	W4 1A00
	W5 2021	W5 0000
Data	0282 0068	Data 0282 0068
	SR 0000	SR 0000
	0000	0

MUL.SU W8, [W9], W0 ; Multiply W8\*[W9]

Example 1:

MUL.SU	Integer 16x16-bit Signed-Unsigned Multiply with Accumulator Destination					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
						Х
Syntax:	{label:}	MUL.SU	Wb,	Ws,		
				[Ws],	А	
				[Ws++],	В	
				[Ws],		
				[++Ws],		
				[Ws],		
Operands:	Wb ∈ [W0 Ws ∈ [W0 ACC ∈ [A,	W15]				
Operation:	signed (WI	o) * unsigned	(Ws) →ACC	C(A or B)		
Status Affected:	None					
Encoding:	1011	1001	0www	w111	Аррр	SSSS
Description:	Description: Performs a 16-bit x 16-bit signed multiply with a 32-bit result, which stored in one of the DSP engine accumulators, ACCA or ACCB. T 32-bit result is sign extended to bit 39 prior to being loaded into the accumulator.					CB. The
	The source operands are treated as integer or fractional values depending upon the operating mode of the DSP engine (as defined by the IF bit in CORCON<0>). The first source operand is interpreted as two's complement signed value and the second source operand is interpreted as an unsigned value.					efined by reted as a
	The 'd' bits The 'p' bits	s select the a s select the ad s select sourc selects the do	ddress of the e Address m	e source regis node 2.	ster.	
		This instructi The state of have no effe	the multiplie	r mode bits (l	JS<1:0> in C	
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-mod	33E and PIC2 dify-write oper ee <b>Note 3</b> in <b>\$</b>	ations on nor	-CPU Specia	al Function R	egisters. For	

Integer 16x16-bit Signed-Unsigned Multiply with
Accumulator Destination

Example 1:	MUL.SU	W8,	W9,	А	
------------	--------	-----	-----	---	--

	Before Instruction		After Instruction
W8	F000	W8	F000
W9	F000	W9	F000
Acc A	00 0000 0000	Acc A	FF F100 0000
SR	0000	SR	0000

MUL.SU	J		16-bit Signe nulator Dest	ed-Unsigned tination	Short Liter	al Multiply	
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
						Х	
Syntax:	{label:}	MUL.SU	Wb,	#lit5,	A B		
Operands:	Wb ∈ [Wi lit5 ∈ [0 ACC ∈ [A	. 31]					
Operation:	signed (W	/b) * unsigned	(lit5) →ACC	(A or B)			
Status Affected:	None						
Encoding:	1011	1001	0www	w111	A11k	kkkk	
	32-bit res accumula The sourd dependin the IF bit two's com	Performs a 16-bit x 16-bit signed multiply with a 32-bit result, which is stored in one of the DSP engine accumulators, ACCA or ACCB. The 32-bit result is sign extended to bit 39 prior to being loaded into the target accumulator. The source operands are treated as integer or fractional values depending upon the operating mode of the DSP engine (as defined by the IF bit in CORCON<0>). The first source operand is interpreted as a two's complement signed value and the second source operand is					
	The 'w' bi The 'k' bit	interpreted as an unsigned value. The 'w' bits select the address of the base register. The 'k' bits select the 5-bit literal value. The 'A' bit selects the destination accumulator for the product.					
	Note 1: 2:	This instructi The state of have no effe	the multiplier	r mode bits (l	JS<1:0> in C		
Words:	1						
Cycles:	1						
Example 1:	MUL.SU W8, #	0x02, A					
	Befor Instruct W8		ا W8	After nstruction 0042	2		

00 0000 0000

0000

Acc A

SR

Integer 16x16-bit Signed-Unsigned Short Literal Multiply
with Accumulator Destination

00 0000 0084

0000

Acc A

SR

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	MUL.US	Wb,	Ws,	Wnd		
				[Ws],			
				[Ws++],			
				[Ws],			
				[++Ws],			
				[Ws],			
Operands:	Wb∈ [W0						
	$Ws \in [W0]$	0 W15] /0, W2, W4	\\\/1 2]				
Operation:	-	(Wb) * signed	-	d:Wnd + 1			
Status Affected:	None	()	(,				
Encoding:	1011	1000	1www	wddd	dppp	SSSS	
	The Wb o and the re integer. Re	and the most perand is inte sult Wnd are egister direct lirect or regist	rpreted as a interpreted a addressing r	n unsigned in as a two's cor must be used	iteger. The W nplement sig for Wb and '	/s operand jned Wnd.	
	The 'w' bit The 'd' bit The 'p' bit	s select the a s select the a s select the s s select the s	ddress of the ddress of the ource Addres	e base regist e lower destir ss mode.	er.		
	Note 1:	This instruct	ion operates	in Word mod	le only.		
	2:						
	3:			nce W15<0>	-	ero.	
	4:	-	d the US<1:0	0> bits in the			
Words:	1						
Cycles:	1 <sup>(1)</sup>						
read-mo	C33E and PIC2 odify-write ope see <b>Note 3</b> in	rations on noi	n-CPU Speci	al Function R	egisters. For		

#### . . . . . ....

Example 1:	MUL.US	W0,	[W1],	W2		ltiply W ore the		•	lgned-signed) 2:W3	)
	-	fore				After				
	Instru	uction				Instructio	n			
١	<i>N</i> 0 C	:000			W0	C000				
١	N1 2	2300			W1	2300				
١	N2 0	0DA			W2	0000				
١	N3 C	C25			W3	F400	1			
Data 23	00 F	000		Data	2300	F000				
:	SR 0	0000			SR	0000				
Example 2:	MUL.US	W6,	[W5++	], W	; ;	Mult. W6 Store th Post-Inc	e resu	Ìt to	gned-signed) W10:W11	
	Be	fore				After				
	Instru	uction				Instructio	n			
١	N5 0	C00			W5	0C02	1			
١	<i>N</i> 6 F	FFF			W6	FFFF				
W	/10 0	908			W10	8001				
W	/11 61	EEB			W11	7FFE				
Data 0C	:00 7	FFF		Data	0C00	7FFF				
:	SR 0	0000			SR	0000	1			

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
						Х
Syntax:	{label:}	MUL.US	Wb,	Ws,	A	
				[Ws],	В	
				[Ws++],		
				[Ws],		
				[++Ws],		
				[Ws],		
Operands:	Wb ∈ [W0 Ws ∈ [W0 ACC ∈ [A,	W15]				
Operation:	unsigned (	Wb) * signed	(Ws) →ACC	C(A or B)		
Status Affected:	None					
Encoding:	1011	1000	0www	w111	Аррр	SSSS
Description:	Dorforme a	16-hit v 16-l	hit signed m	ultiply with a '	32-bit result	which is
Description:	stored in o	ne of the DS It is sign exte	P engine ac	ultiply with a 3 cumulators, A 9 prior to beir	CCA or ACC	B. The
Description:	stored in o 32-bit resu accumulat The source depending the IF bit ir unsigned v	ne of the DS It is sign exte or. e operands a upon the op n CORCON<	P engine acc nded to bit 3 re treated as erating mode 0>). The firs second sou	cumulators, A	ACCA or ACC ng loaded into actional value engine (as d and is interp	CB. The o the targe es efined by reted as a
Description:	stored in o 32-bit resu accumulate The source depending the IF bit ir unsigned v compleme The 'w' bits The 'd' bits The 'p' bits	ne of the DS It is sign exte or. e operands a upon the op r CORCON value and the nt signed values s select the a s select the a s select sources	P engine acc nded to bit 3 re treated as erating mode 0>). The firs second sou ue. ddress of the ddress of the ce Address n	s integer or fra of the DSP t source oper rce operand i e base registe source registe	ACCA or ACC ng loaded into actional value engine (as d and is interpr is interpreted er. ster.	CB. The o the targe es efined by reted as a as a two's
Description:	stored in o 32-bit resu accumulate The source depending the IF bit ir unsigned v compleme The 'w' bits The 'd' bits The 'A' bit Note 1:	ne of the DS It is sign exter or. e operands a upon the op of CORCON	P engine acc nded to bit 3 re treated as erating mode 0>). The firs second sou ue. ddress of the ddress of the e Address n estination ac on operates the multiplie	s integer or fra of the DSP t source oper rce operand i e base registe source registe source registe source registe source registe	ACCA or ACC ng loaded into actional value engine (as d and is interprise is interpreted er. ster. r the product de only. US<1:0> in C	CB. The o the targe es efined by reted as a as a two's CORCON)
Description:	stored in o 32-bit resu accumulate The source depending the IF bit ir unsigned v compleme The 'w' bits The 'd' bits The 'A' bit Note 1:	ne of the DS It is sign exter or. e operands a upon the op of CORCON	P engine acc nded to bit 3 re treated as erating mode 0>). The firs second sou ue. ddress of the ddress of the e Address n estination ac on operates the multiplie	cumulators, A 9 prior to beir s integer or fra e of the DSP t source oper rce operand i e base registe source regis node 2. ccumulator fo in Word moo r mode bits (I	ACCA or ACC ng loaded into actional value engine (as d and is interprise is interpreted er. ster. r the product de only. US<1:0> in C	CB. The o the target es efined by reted as a as a two's CORCON)

details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

### Integer 16x16-bit Unsigned-Signed Multiply with

	Before Instruction		After Instruction
W0	C000	W0	0000
W1	F000	W1	F000
Acc B	00 0000 0000	Acc B	FF F400 0000
SR	0000	SR	0000

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	MUL.UU	Wb,	#lit5,	Wnd	
Operands:	Wb ∈ [W0 lit5 ∈ [0 Wnd ∈ [W	-	. W12]			
Operation:	unsigned	(Wb) * unsigne	ed lit5 →Wnr	d:Wnd + 1		
Status Affected:	None					
Encoding:	1011	1000	0www	wddd	d11k	kkkk
	the result register), a Both oper Register d The 'w' bit The 'd' bit	wo successive is stored in W and the most s rands and the direct addressi ts select the ac s select the ac	/nd (which mi significant wo result are intr ing must be u address of the ddress of the	ust be an even ord of the resisterpreted as u used for Wb e base register olower destin	en numbered sult is stored ir unsigned inte and Wnd. ter. nation registe	d working in Wnd + 1. egers.
		s define a 5-bi This instruction	U	U		
	2: 3: 4:	Since the pro an even work how double v Wnd may not	oduct of the n king register. words are ali ot be W14, sir d the US<1:0	multiplication . See Figure igned in mem nce W15<0> D> bits in the 0	is 32 bits, Wr 4-3 for inform nory.	mation on ero.
Words:	1					
Cycles:	1					
Example 1: MU W1 W1 SI	Before Instruction /0 2323 .2 4512 .3 7821	0xF, W12 ; ; W W1 W1 SI	Store the After Instruction (0 2323 L2 0F0D L3 0002	result to N		
Example 2: ML	UL.UU W7, #0		Multiply W Store the			
W W W	/1 3805	W W W	/1 001D	I		

# 

Instruction Descriptions

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	MUL.UU	Wb,	Ws,	Wnd				
				[Ws],					
				[Ws++],					
				[Ws],					
				[++Ws],					
				[Ws],					
Operands:	Wb ∈ [W0 Ws ∈ [W0 Wnd ∈ [W		W12]						
Operation:	unsigned (	(Wb) * unsign	ed (Ws) →W	/nd:Wnd + 1					
Status Affected:	None								
Encoding:	1011	1000	0www	wddd	dppp	SSSS			
Description:	Multiply the contents of Wb with the contents of Ws, and store the a result in two successive working registers. The least significant wo the result is stored in Wnd (which must be an even numbered worl register), and the most significant word of the result is stored in Wnd + 1. Both source operands and the result are interpreted as unsigned integers. Register direct addressing must be used for Wt Wnd. Register direct or indirect addressing may be used for Ws.								
	The 'w' bits select the address of the base register. The 'd' bits select the address of the lower destination register. The 'p' bits select the source Address mode. The 's' bits select the source register.								
	Note 1:	This instructi	on operates	in Word mod	de only.				
	2:	Since the pro an even work how double v	king register.	See Figure	4-3 for inform				
	3:	Wnd may no		-	-	ero.			
	4:	The IF bit and no effect on t			CORCON re	gister have			
Words:	1								
Cycles:	1(1)								

read-modify-write operations on non-CPU Special Function Registers. For more details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

	,	; Store	e the res	sult to W2:W3
W0 W2 W3 W4 SR	Before Instruction FFFF 2300 00DA FFFF 0000	W0 W2 W3 W4 SR	After Instruction FFFF 0001 FFFE FFFF 0000	l
Example 2: MUL	.UU W0,	; St	-	[W1] (unsigned-unsigned) result to W4:W5 ement W1
	Before		After	
	Instructior	1	Instructior	ı
W0	1024	W0	1024	
W1	2300	W1	2302	
W4	9654	W4	6D34	
W5	BDBC	W5	0D80	
Data 2300	D625	Data 2300	D625	
SR	0000	SR	0000	

MUL.UU W4, W0, W2 ; Multiply W4\*W0 (unsigned-unsigned)

5

Example 1:

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
implementeu m.	FIC24F	FIC24H	FIC24E	USFICSUF	USFIC33F	X
						~
Syntax:	{label:}	MUL.UU	Wb,	Ws,	A	
				[Ws],	В	
				[Ws++],		
				[Ws],		
				[++Ws],		
				[Ws],		
Operands:	Wb∈[W0	) W15]				
	Ws ∈ [W0 ACC ∈ [A	W15]				
Operation:	unsigned	(Wb) * unsign	ed (Ws) →A	CC(A or B)		
Status Affected:	None					
Encoding:	1011	1000	0www	w111	Аррр	SSSS
Description:	stored in c	a 16-bit x 16- one of the DS ult is zero exte umulator.	P engine ac	cumulators, A	ACCA or ACC	B. The
	depending	e operands a g upon the op n CORCON< values.	erating mode	e of the DSP	engine (as d	efined by
	The 'd' bits The 'p' bits	s select the a s select the a s select sourc selects the d	ddress of the e Address n	e source regis node 2.	ster.	
	Note 1: 2:		the multiplie	in Word mod r mode bits ( operation of t	US<1:0> in C	
Words:	1					
	1 <sup>(1)</sup>					
Cycles:	1. ,					

Example 1: MUL.UU W4, W0, B

	Before Instruction		After Instruction
W0	FFFFF	W0	FFFFF
W4	FFFFF	W4	FFFFF
Acc B	00 0000 0000	Acc B	FF FFFE 0001
SR	0000	SR	0000

MUL.UU	Integer 16x16-bit Unsigned Short Literal Multiply with Accumulator Destination								
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33			
						Х			
Syntax:	{label:}	MUL.UU	Wb,	#lit5,	A B				
Operands:	Wb ∈ [W0 lit5 ∈ [0 ACC ∈ [A,	31]							
Operation:	unsigned (Wb) * unsigned (lit5) $\rightarrow$ ACC(A or B)								
Status Affected:	None								
Encoding:	1011	1000	0www	w111	A11k	kkkk			
Description:	Performs a 16-bit x 16-bit signed multiply with a 32-bit result, which is stored in one of the DSP engine accumulators, ACCA or ACCB. The 32-bit result is zero extended to bit 39 prior to being loaded into the target accumulator. The source operands are treated as integer or fractional values depending upon the operating mode of the DSP engine (as defined by the IF bit in CORCON<0>). Both source operands are treated as unsigned values.								
	The 'w' bits select the address of the base register. The 'k' bits select the 5-bit literal. The 'A' bit selects the destination accumulator for the product.								
	<ol> <li>Note 1: This instruction operates in Word mode only.</li> <li>2: The state of the multiplier mode bits (US&lt;1:0&gt; in CORCON) have no effect upon the operation of this instruction.</li> </ol>								
Words:	1								
Cycles:	1								
Example 1: MUL.	UU W8, #G	)x02, A							
W8		on 0042	W8	After Instruction 004					
Acc A SR	00 0000	0000	Acc A SR	800 0000 008 000					

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
			Х			Х			
Syntax:	{label:}	MULW.SS	Wb,	Ws,	Wnd				
				[Ws],					
				[Ws++],					
				[Ws],					
				[++Ws],					
				[Ws],					
Operands:	Wb ∈ [W0	-							
	Ws ∈ [W0 W15] Wnd ∈ [W0, W2, W4 W12]								
Operation:	-	b) * signed (\	-						
Status Affected:	None	,							
Encoding:	1011	1001	1www	wddd	dppp	SSSS			
	for Wb and Wnd. Register direct or register indirect addressing may be used for Ws. The 'w' bits select the address of the base register. The 'd' bits select the address of the lower destination register. The 'p' bits select the source Address mode. The 's' bits select the source register.								
	Note 1:		•	in Word mod	te only				
	2:	Wnd must b	•		-				
	<b>3:</b> Wnd may not be W14, since W15<0> is fixed to zero.								
	4:			0> bits in the	CORCON re	gister have			
		no eneci on							
Words.	1		this operatio	11.					
Words: Cvcles:	1 1 <sup>(1)</sup>		uns operatio	"".					
Cycles: Note 1: In dsPIC3: read-modi	1 <sup>(1)</sup> 3E and PIC2 fy-write ope	24E devices, r rations on nor Section 3.2.1	he listed cyc n-CPU Speci	le count does al Function R	egisters. For				
Cycles: Note 1: In dsPIC3 read-modi details, se	1 <sup>(1)</sup> 3E and PIC2 fy-write ope	24E devices, r rations on nor <b>Section 3.2.1</b> v1, W12 ;	he listed cyc n-CPU Speci . <b>"Multi-Cyc</b> Multiply W	le count does al Function R le Instruction	egisters. For ns".				
Cycles: <b>Note 1:</b> In dsPIC3: read-modi details, ser <u>Example 1:</u> MULW	1 <sup>(1)</sup> BE and PIC2 fy-write ope e <b>Note 3</b> in	24E devices, r rations on nor <b>Section 3.2.1</b> v1, W12 ;	he listed cyc n-CPU Speci . <b>"Multi-Cyc</b> Multiply W	le count does al Function R <b>le Instructio</b> 0*W1 result to N	egisters. For ns".				

W12

SR

D314

0000

W12

SR

FFFF
Example 2: MUL	W.SS W2,	, [W4], WO	; Multip	crement W4 ly W2*[W4] the result to W0
	Before Instruction	I	After Instructio	n
W0	FFFF	W	28F8	
W2	0045	W2	0045	
W4	27FE	W2	27FC	]
Data 27FC	0098	Data 27FC	: 0098	

SR

SR

MULW.SU		Integer 16x Result	16-bit Signe	ed-Unsigned	l Multiply wi	th 16-bit
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			х			Х
Syntax:	{label:}	MUL.SU	Wb,	Ws,	Wnd	
,	, ,			[Ws],		
				[Ws++],		
				[Ws],		
				[++Ws],		
				[Ws],		
Operands:	Wb∈ [W0 Ws∈ [W0 Wnd∈ [W		W12]			
Operation:	signed (W	b) * unsigned	(Ws) →Wnd			
Status Affected:	None					
Encoding:	1011	1001	0www	wddd	dppp	SSSS
	unsigned i Wnd. Regi The 'w' bit The 'd' bits The 'p' bits	nt signed inte nteger. Regis ster direct or s select the a s select the ac s select the so s select the so	ter direct add register indir ddress of the ddress of the purce Addres	dressing mus ect addressi base registe lower destin s mode.	st be used for ng may be u er.	r Wb and sed for Ws
	Note 1: 2: 3: 4:	This instructi Wnd must be Wnd may no The IF bit and	e an even wo t be W14, sir d the US<1:0	orking registe nce W15<0> )> bits in the (	r. is fixed to ze	
Words:	1	no effect on t	ins operation	1.		
Cycles:	1 1(1)					
Note 1: In dsPIC33 read-modif	BE and PIC2	4E devices, t ations on nor Section 3.2.1	I-CPU Specia	al Function R	egisters. For	
Example 1: MULW	.SU W8, [	W9], W0		y W8*[W9] he result	to WO	
lr W0 W8 W9 Data 178C SR	Before astruction 68DC F000 178C F000 0000	W W W Data 178 S	8 F000 9 178C C F000	I		

Example 2: MUL	W.SU W2,	,	Nultiply	
	Before		After	
	Instruction		Instructior	ו
W2	0040	W2	0040	
W3	0280	W3	0282	
W4	1819	W4	1A00	
Data 0282	0068	Data 0282	0068	
SR	0000	SR	0000	

MULW.SU	J	Integer 16x with 16-bit		ed-Unsigned	I Short Liter	al Multiply
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	MULW.SU	Wb,	#lit5,	Wnd	
Operands:	Wb ∈ [W0 lit5 ∈ [0					
	Wnd ∈ [W	/0, W2, W4	W12]			
Operation:	signed (W	b) * unsigned	(lit5) →Wnd			
Status Affected:	None	-	1			
Encoding:	1011	1001	0www	wddd	d11k	kkkk
	The Wb o	ng register, wh perand and th ent signed inte /nd.	ne result Wno	d are interpre	eted as a two	'S
	The 'd' bit	s select the a s select the a s select the 5	ddress of the	e lower destir		r.
	Note 1:	This instruct	ion operates	in Word mod	de only.	
	2:	Wnd must be				
	3: 4:	Wnd may no The IF bit an no effect on	d the US<1:0	)> bits in the		
Words:	1					
Cycles:	1					
Example 1: MU	LW.SU W8, ≉	≠0×04, W0		Ly W8 * #0x0 the result		
WC WE SF	3 1000		After Instruction /0 4000 /8 1000 R 0000	I		

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			X			Х
Syntax:	{label:}	MULW.US	Wb,	Ws,	Wnd	
Cymux.	ງານວະ,		vv.,	Ws, [Ws],	VVIIG	
				[₩S], [WS++],		
				[vvs++], [Ws],		
				[vvs], [++Ws],		
				[++vvs], [Ws],		
				[ •••],		
Operands:	$Wb \in [W0]$					
	$Ws \in [W0]$ Wnd $\in [W0]$	W15] 0, W2, W4	W12]			
Operation:		Wb) * signed		l		
Status Affected:	None	VV.,	()			
Encoding:	1011	1000	1www	wddd	dppp	SSSS
Description:	-	e contents of				
Decompact	in a workin	g register, wh	nich must be	an even num	nbered workir	ng register.
	The Wb op	perand is inter	rpreted as ar	n unsigned in	iteger. The W	/s operand
	and the res	sult Wnd are i	interpreted a	is a two's cor	nplement sig	ned
	integer. Re	egister direct a	addressing n	nust be used	for Wb and V	Wnd.
					ly be used for	
	rtogiotor a	inect of regist	ci muncei at	an cooling ma	ly be used to	
	The 'w' bits	s select the a	ddress of the	e base registe	er.	
	The 'w' bits	s select the a s select the ac	ddress of the ddress of the	e base registe lower destin	er.	
	The 'w' bits The 'd' bits The 'p' bits	s select the ac s select the ac s select the sc	ddress of the ddress of the ource Addres	e base registe lower destin ss mode.	er.	
	The 'w' bits The 'd' bits The 'p' bits The 's' bits	s select the ac s select the ac s select the so s select the so	ddress of the ddress of the ource Addres ource registe	e base registe lower destin ss mode. r.	er. nation registe	
	The 'w' bits The 'd' bits The 'p' bits The 's' bits <b>Note 1:</b>	s select the ac select the ac select the so select the so select the so This instruction	ddress of the ddress of the burce Addres burce registe on operates	e base registe lower destin ss mode. r. in Word mod	er. nation registe le only.	
	The 'w' bits The 'd' bits The 'p' bits The 's' bits Note 1: 2:	s select the ac s select the ac s select the so s select the so This instruction Wnd must be	ddress of the ddress of the burce Addres burce registe on operates e an even wo	e base registe lower destin ss mode. r. in Word mod prking registe	er. nation registe le only. r.	r.
	The 'w' bits The 'd' bits The 'p' bits The 's' bits Note 1: 2: 3:	s select the ac s select the ac s select the so s select the so This instruction Wnd must be Wnd may no	ddress of the ddress of the burce Addres burce registe on operates e an even wo t be W14, sin	e base registe lower destin ss mode. r. in Word mod orking registe nce W15<0>	er. hation registe le only. hr. is fixed to ze	r. Pro.
	The 'w' bits The 'd' bits The 'p' bits The 's' bits Note 1: 2: 3: 4:	s select the ac s select the ac s select the so s select the so This instruction Wnd must be	ddress of the ddress of the burce Addres burce registe on operates e an even wo t be W14, sin d the US<1:0	e base regista e lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the 0	er. hation registe le only. hr. is fixed to ze	r. Pro.
Words:	The 'w' bits The 'd' bits The 'p' bits The 's' bits Note 1: 2: 3: 4:	s select the ac select the ac select the so select the so This instruction Wnd must be Wnd may no The IF bit and	ddress of the ddress of the burce Addres burce registe on operates e an even wo t be W14, sin d the US<1:0	e base regista e lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the 0	er. hation registe le only. hr. is fixed to ze	r. Pro.
Words: Cycles:	The 'w' bits The 'd' bits The 'p' bits The 's' bits Note 1: 2: 3: 4:	s select the ac select the ac select the so select the so This instruction Wnd must be Wnd may no The IF bit and	ddress of the ddress of the burce Addres burce registe on operates e an even wo t be W14, sin d the US<1:0	e base regista e lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the 0	er. hation registe le only. hr. is fixed to ze	r. Pro.
Cycles: Note 1: In dsPIC33	The 'w' bits The 'd' bits The 'p' bits The 's' bits Note 1: 2: 3: 4: 1 1(1) 3E and PIC2	s select the ac s select the ac s select the so s select the so This instruction Wnd must be Wnd may not The IF bit and no effect on t	ddress of the ddress of the ource Addres ource registe on operates e an even wo t be W14, sin d the US<1:0 this operation he listed cycl	e base registe lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the ( n. le count does	er. lation registe le only. r. is fixed to ze CORCON reg	r. ero. gister have read and
Cycles: Note 1: In dsPIC33 read-modif	The 'w' bits The 'd' bits The 'p' bits The 's' bits Note 1: 2: 3: 4: 1 1(1) 3E and PIC2 fy-write oper	s select the ac s select the ac s select the so s select the so This instruction Wnd must be Wnd may not The IF bit and no effect on t	ddress of the ddress of the burce Addres burce registe on operates e an even wo t be W14, sin d the US<1:0 this operation he listed cycl h-CPU Specia	e base registe lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the 0 n. le count does al Function R	er. lation register le only. r. is fixed to ze CORCON reg not apply to egisters. For	r. ero. gister have read and
Cycles: Note 1: In dsPIC33 read-modif	The 'w' bits The 'd' bits The 'p' bits The 's' bits Note 1: 2: 3: 4: 1 1(1) 3E and PIC2 fy-write oper	s select the ac s select the ac s select the so select the so This instruction Wnd must be Wnd may not The IF bit and no effect on t	ddress of the ddress of the burce Addres burce registe on operates e an even wo t be W14, sin d the US<1:0 this operation he listed cycl h-CPU Specia	e base registe lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the 0 n. le count does al Function R	er. lation register le only. r. is fixed to ze CORCON reg not apply to egisters. For	r. ero. gister have read and
Cycles: Note 1: In dsPIC33 read-modif details, see	The 'w' bits The 'd' bits The 'd' bits The 's' bits Note 1: 2: 3: 4: 1 1(1) 3E and PIC2 fy-write oper e Note 3 in S	s select the ac s select the ac s select the so this instruction Who must be Who may not The IF bit and no effect on t 24E devices, th ations on non Section 3.2.1	ddress of the ddress of the burce Addres burce registe on operates e an even wo t be W14, sin d the US<1:C this operation he listed cycl -CPU Specia "Multi-Cycl Multiply W0	e base registe lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the ( n. le count does al Function R <b>e Instructior</b>	er. lation register le only. r. is fixed to ze CORCON reg s not apply to egisters. For ns". igned-signe	r. ero. gister have read and more
Cycles: <b>Note 1:</b> In dsPIC33 read-modif details, see <u>Example 1:</u> MULW	The 'w' bits The 'd' bits The 'd' bits The 's' bits Note 1: 2: 3: 4: 1 1(1) 3E and PIC2 fy-write oper e Note 3 in S	s select the ac s select the ac s select the so this instruction Who must be Who may not The IF bit and no effect on t 24E devices, th ations on non Section 3.2.1	ddress of the ddress of the burce Address ource registe on operates e an even wo t be W14, sin d the US<1:C this operation he listed cycl o-CPU Specia <b>"Multi-Cycl</b> Multiply W0 Store the r	e base registe lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the ( n. le count does al Function R <b>e Instruction</b> *[W1] (uns:	er. lation register le only. r. is fixed to ze CORCON reg s not apply to egisters. For ns". igned-signe	r. ero. gister have read and more
Cycles: <b>Note 1:</b> In dsPIC33 read-modif details, see <u>Example 1:</u> MULW	The 'w' bits The 'd' bits The 'd' bits The 's' bits Note 1: 2: 3: 4: 1 1(1) 3E and PIC2 fy-write oper e Note 3 in S	s select the ac s select the ac s select the so this instruction Who must be Who may not The IF bit and no effect on t 24E devices, th ations on non Section 3.2.1	ddress of the ddress of the burce Addres burce registe on operates e an even wo t be W14, sin d the US<1:C this operation he listed cycl -CPU Specia "Multi-Cycl Multiply W0	e base registe lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the ( n. le count does al Function R <b>e Instructior</b> *[W1] (uns: esult to W2	er. lation register le only. r. is fixed to ze CORCON reg s not apply to egisters. For ns". igned-signe	r. ero. gister have read and more
Cycles: <b>Note 1:</b> In dsPIC33 read-modif details, see <u>Example 1:</u> MULW	The 'w' bits The 'd' bits The 'd' bits The 's' bits Note 1: 2: 3: 4: 1 1(1) 3E and PIC2 fy-write oper e Note 3 in S	s select the ac s select the ac s select the so this instruction Who must be Who may not The IF bit and no effect on t 24E devices, th ations on non Section 3.2.1	ddress of the ddress of the burce Address ource registe on operates e an even wo t be W14, sin d the US<1:C this operation he listed cycl i-CPU Specia "Multi-Cycl Bultiply W0 Store the r After Instruction	e base registe lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the ( n. le count does al Function R <b>e Instructior</b> *[W1] (uns: esult to W2	er. lation register le only. r. is fixed to ze CORCON reg s not apply to egisters. For ns". igned-signe	r. ero. gister have read and more
Cycles: <b>Note 1:</b> In dsPIC33 read-modif details, see <u>Example 1:</u> MULW	The 'w' bits The 'd' bits The 'd' bits The 's' bits Note 1: 2: 3: 4: 1 1(1) 3E and PIC2 fy-write oper e Note 3 in S 7.US W0, [ Before nstruction	s select the ac s select the ac s select the so s select the so This instruction Wnd must be Wnd may not The IF bit and no effect on t 44E devices, the ations on non Section 3.2.1 w1], w2 ; M ; S	ddress of the ddress of the burce Address ource registe on operates e an even wo t be W14, sin d the US<1:C this operation he listed cycl -CPU Specia "Multi-Cycl Multiply W0 Store the r After Instruction 0 C000	e base registe lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the ( n. le count does al Function R <b>e Instructior</b> *[W1] (uns: esult to W2	er. lation register le only. r. is fixed to ze CORCON reg s not apply to egisters. For ns". igned-signe	r. ero. gister have read and more
Cycles: <b>Note 1:</b> In dsPIC33 read-modif details, see <u>Example 1:</u> MULW In W0	The 'w' bits The 'd' bits The 'd' bits The 's' bits Note 1: 2: 3: 4: 1 1(1) 3E and PIC2 fy-write oper e Note 3 in S 7. US W0, [ Before nstruction C000	s select the ac s select the ac s select the so this instruction Wind must be Wind may not The IF bit and no effect on t section 3.2.1 W1], W2 ; M ; S	ddress of the ddress of the burce Address ource registe on operates e an even wo t be W14, sin d the US<1:C this operation he listed cycl o-CPU Specia <b>"Multi-Cycl</b> Multiply W0 Store the r After Instruction 0 <u>C000</u> 1 2300	e base registe lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the ( n. le count does al Function R <b>e Instructior</b> *[W1] (uns: esult to W2	er. lation register le only. r. is fixed to ze CORCON reg s not apply to egisters. For ns". igned-signe	r. ero. gister have read and more
Cycles: <b>Note 1:</b> In dsPIC33 read-modif details, see <u>Example 1:</u> MULW In W0 W1	The 'w' bits The 'd' bits The 'd' bits The 's' bits Note 1: 2: 3: 4: 1 1(1) 3E and PIC2 fy-write oper e Note 3 in § 7.US W0, [ Before nstruction C000 2300	s select the ac s select the ac s select the so s select the so This instruction Wnd must be Wnd may not The IF bit and no effect on t section 3.2.1 W1], W2 ; M ; S	ddress of the ddress of the ource Address ource registe on operates e an even wo t be W14, sin d the US<1:C this operation he listed cycl o-CPU Specia "Multi-Cycl Multiply W0 Store the r After Instruction 0 C000 1 2300 2 0000	e base registe lower destin ss mode. r. in Word mod orking registe nce W15<0> )> bits in the ( n. le count does al Function R <b>e Instructior</b> *[W1] (uns: esult to W2	er. lation register le only. r. is fixed to ze CORCON reg s not apply to egisters. For ns". igned-signe	r. ero. gister have read and more

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Instruction Descriptions

Example 2: MUL	W.US W6,		; Store	W6*[W5] (unsigned-signed) the result to W10 ncrement W5
	Before		After	
	Instruction		Instruction	า
W5	0C00	W5	0C02	
W6	FFFF	W6	FFFF	
W10	0908	W10	8001	
Data 0C00	7FFF	Data 0C00	7FFF	
SR	0000	SR	0000	

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	MULW.UU	Wb,	Ws,	Wnd	
				[Ws],		
				[Ws++],		
				[Ws],		
				[++Ws],		
				[Ws],		
Operands:	Wb∈ [W0					
• F =	Ws ∈ [W0	) W15]				
	-	/0, W2, W4	-			
Operation:	unsigned (	(Wb) * unsign	ied (Ws) →	√nd		
Status Affected:	None					
Encoding:	1011	1000	0www	wddd	dppp	SSSS
	register). B unsigned in Wnd. Regis The 'w' bits The 'd' bits The 'p' bits	ng registers, v Both source o integers. Regi ister direct or is select the a s select the ac s select the so s select the so	pperands and jister direct a r indirect add address of the address of the source Addres	d the result an addressing mu Iressing may le base regist e lower destir less mode.	re interpretec ust be used f be used for V ter.	d as for Wb and Ws.
			-	s in Word mod	de only.	
			-	orking registe	-	
				ince W15<0>		۹rO
				0> bits in the		
			this operatio		00	3.0.2
Words:	1					
Cycles:	1 <sup>(1)</sup>					
	fy-write oper	24E devices, t rations on nor <b>Section 3.2.1</b>	n-CPU Speci	ial Function R	Registers. For	
Example 1: MULW.	.UU W4, W	WO, W2 ; Mul ; Sto	ltiply W4*W ore the res		d-unsigned)	)
	Before nstruction FFFF 2300		After Instructior V0 FFFF V2 0001	n ]		

Instruction Descriptions

MULW.U	U	Integer 16x 16-bit Resu		gned Short I	Literal Multi	oly with
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	MULW.UU	Wb,	#lit5,	Wnd	
Operands:	Wb ∈ [W0 lit5 ∈ [0 Wnd ∈ [M		W12]			
Operation:	unsigned	(Wb) * unsign	ed →Wnd			
Status Affected:	None					
Encoding:	1011	1000	0www	wddd	d11k	kkkk
	The 'd' bit	ts select the a s select the a s select the 5-	ddress of the	e lower destir		er.
	Note 1:	This instructi	on operates	in Word mod	de only.	
	2:	Wnd must be		• •		
	3:	Wnd may no				
	4:	The IF bit and no effect on t			CORCON re	gister nave
Words:	1					
Cycles:	1					
Example 1: M	ULW.UU W4,	#0x04, W2		ly W4*W0 (ι the result	ınsigned-un to W2	signed)
	Before		After			
	Instruction		Instruction	1		

1000

	Before	
I	nstructior	ו ו
W2	2300	W2
W4	1000	W4
SR	0000	SR

NEG		Negate f				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	NEG{.B}	f	{,WREG}		
Operands:	f∈ [0 81	.91]				
Operation:	(f) + 1 →de	estination des	signated by D	)		
Status Affected:	DC, N, OV	, Z, C				
Encoding:	1110	1110	0BDf	ffff	ffff	ffff
Description:	place the red determines stored in W register.	he two's com esult in the d the destinat /REG. If WRF	estination re- ion register. EG is not spe	gister. The op If WREG is s ecified, the re	otional WRE pecified, the sult is stored	G operand result is I in the file
	The 'D' bit	selects byte of selects the d select the ad	estination ('@	)' for WREG,		
		The extension rather than a denote a wor	word operat	tion. You may	/usea.We	
	2:	The WREG i	is set to work	king register \	N0.	
Words:	1					
Cycles:	1 <sup>(1)</sup>					
Cycles: Note 1: In dsPIC33 read-modi	1 <sup>(1)</sup> 3E and PIC2 fy-write oper e <b>Note 3</b> in S	4E devices, t ations on nor Section 3.2.1 WREG ; Neg ; Sto	n-CPU Specia . " <mark>Multi-Cycl</mark>	al Function R e Instruction	egisters. For 1 <b>s</b> ".	
Cycles: <b>Note 1:</b> In dsPIC3: read-modir details, set <u>Example 1:</u> NEG.	1 <sup>(1)</sup> 3E and PIC2 fy-write oper e <b>Note 3</b> in S	ations on nor Section 3.2.1 WREG ; Neg ; Sto ; Sto WREG (W0) Data 0880 SF	n-CPU Specia "Multi-Cycl gate (0x880 pre result After Instruction ) 90AB 0 2355 0 0008 (N	al Function R e Instruction	egisters. For I <b>s</b> ". de)	
Cycles: Note 1: In dsPIC33 read-modi details, set Example 1: NEG. WREG (W0) Data 0880 SR Example 2: NEG Ir Data 1200 SR	1 <sup>(1)</sup> 3E and PIC2 fy-write oper e <b>Note 3</b> in S B 0x880, Before istruction 9080 2355 0000	ations on nor Section 3.2.1 WREG ; Neg ; Sto ; Sto WREG (W0) Data 0880 SF	A-CPU Specia <b>"Multi-Cycl</b> gate (0x886 pre result After Instruction ) 90AB 2355 2008 (N gate (0x120 After Instruction ) 76DD	al Function R e Instruction ) (Byte mon to WREG	egisters. For I <b>s</b> ". de)	
Cycles: Note 1: In dsPIC3: read-modi details, set Example 1: NEG. Ir WREG (W0) Data 0880 SR Example 2: NEG Ir Data 1200	1 <sup>(1)</sup> 3E and PIC2 fy-write oper e <b>Note 3</b> in <b>S</b> B 0x880, Before instruction 9080 2355 0000 0x1200 Before instruction 8923	ations on nor Section 3.2.1 WREG ; Neg ; Sto WREG (W0) Data 0880 SF ; Neg Data 1200	A-CPU Specia <b>"Multi-Cycl</b> gate (0x886 pre result After Instruction ) 90AB 2355 2008 (N gate (0x126 After Instruction ) 76DD	al Function R e Instruction ) (Byte mon to WREG	egisters. For I <b>s</b> ". de)	
Cycles: Note 1: In dsPIC33 read-modi details, set Example 1: NEG. WREG (W0) Data 0880 SR Example 2: NEG Ir Data 1200 SR	1 <sup>(1)</sup> 3E and PIC2 fy-write oper e <b>Note 3</b> in <b>S</b> B 0x880, Before instruction 9080 2355 0000 0x1200 Before instruction 8923	ations on nor Section 3.2.1 WREG ; Neg ; Sto WREG (W0) Data 0880 ; Neg Data 1200 SF	A-CPU Specia <b>"Multi-Cycl</b> gate (0x886 pre result After Instruction ) 90AB 2355 2008 (N gate (0x126 After Instruction ) 76DD	al Function R e Instruction ) (Byte mon to WREG	egisters. For I <b>s</b> ". de)	
Cycles: Note 1: In dsPIC33 read-modi details, set Example 1: NEG. WREG (W0) Data 0880 SR Example 2: NEG Ir Data 1200 SR EXAMPLE 2: NEG	1 <sup>(1)</sup> 3E and PIC2 fy-write oper e <b>Note 3</b> in <b>S</b> B 0x880, Before nstruction 9080 2355 0000 0x1200 Before nstruction 8923 0000	ations on nor Section 3.2.1 WREG ; Neg ; Sto WREG (W0) Data 0880 ; Neg Data 1200 SF Negate Ws	A-CPU Specia <b>"Multi-Cycl</b> gate (0x886 pre result After Instruction ) 90AB 2355 0008 (N gate (0x126 After Instruction 0 76DD 0 0000	al Function R e Instruction ) (Byte mon to WREG N = 1) 0) (Word mon	egisters. For Is". de )	more

NEG		Negate Ws				
			[Ws++],	[Wd++]		
			[Ws],	[Wd]		
			[++Ws],	[++Wd]		
			[Ws],	[Wd]		
Operands:	Ws ∈ [W0 Wd ∈ [W0	-				
Operation:	(Ws) + 1 –	→Wd				
Status Affected:	DC, N, OV	, Z, C				
			0.0	qddd	dppp	SSSS
Encoding:	1110 Compute t	1010	0Bqq			
Encoding: Description:	Compute t and place or indirect	he two's com the result in t addressing n	plement of the destination of th	ne contents of on register We for both Ws a	f the source r d. Either regi and Wd.	egister Wasser Ster direct
•	Compute ti and place or indirect The 'B' bit The 'q' bits The 'd' bits The 'p' bits	he two's com the result in t addressing n selects byte	plement of the he destination nay be used or word oper estination Accestination re pource Addre	ne contents of on register We for both Ws a ration ('0' for ddress mode. gister. ss mode.	f the source r d. Either regi and Wd. word, '1' for l	egister Ws ster direct
•	Compute ti and place or indirect The 'B' bit The 'q' bits The 'q' bits The 'q' bits The 's' bits Note: T	he two's com the result in t addressing n selects byte select the de select the de select the se select the se select the se he extension ather than a v	plement of the he destination nay be used or word oper estination Ac estination re burce Addre burce register . B in the ir vord operation	ne contents of on register We for both Ws a ration ('0' for ddress mode. gister. ss mode.	the source r d. Either regi and Wd. word, '1' for l notes a byte o use a	egister Ws ster direct byte).
•	Compute ti and place or indirect The 'B' bit The 'q' bits The 'q' bits The 'g' bits The 's' bits Note: T	he two's com the result in t addressing n selects byte select the de select the de select the se select the se select the se he extension ather than a v	plement of the he destination nay be used or word oper estination Ac estination re burce Addre burce register . B in the ir vord operation	ne contents of on register We for both Ws a ration ('0' for y ddress mode. gister. ss mode. er. hstruction den on. You may u	the source r d. Either regi and Wd. word, '1' for l notes a byte o use a	egister Ws ster direct byte).

Note 1: In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1: NEG.B W3, [W4++] ; Negate W3 and store to [W4] (Byte mode)
; Post-increment W4

I	Before nstructior	ו I	After nstruction	
W3	7839	W3	7839	
W4	1005	W4	1006	
Data 1004	2355	Data 1004	C755	
SR	0000	SR	0008 (N = 1)	
Example 2: NEG	[W2++],	; Negat	lecrement W4 (Word mod e [W2] and store to [ increment W2	
	Before		After	

	Before		After
I	nstructior	ו ו	nstruction
W2	0900	W2	0902
W4	1002	W4	1000
Data 0900	870F	Data 0900	870F
Data 1000	5105	Data 1000	78F1
SR	0000	SR	0000

NEG		Negate Acc	cumulator			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
				Х	Х	Х
Syntax:	{label:}	NEG	Acc			
Operands:	Acc ∈ [A,B	3]				
Operation:	<u> If (Acc = A</u>	<u>):</u>				
	-ACCA - <u>Else:</u> -ACCB -					
Status Affected:	OA, OB, O	AB, SA, SB,	SAB			
Encoding:	1100	1011	A001	0000	0000	0000
Description:	accumulate		s of the Sati	he contents c uration mode ulator.		
	The 'A' bit	specifies the	selected acc	cumulator.		
Words:	1					
Cycles:	1					
Example 1: NEG	; S	egate ACCA tore result ORCON = 0x6		turation)		
	Before			After		
_	Instructio	on	-	Instructio		
ACCA	00 3290 9		ACCA	FF CD6F A		
CORCON SR		0000	CORCON SR		0000	
Example 2: NEG	B ; N ; S	egate ACCB tore result	to ACCB	l saturatio		
	Before			After		
	Instructio		1005 I	Instructio		
ACCB CORCON	FF F230 1		ACCB CORCON	00 0DCF E	EF24 00C0	
SR		0000	SR		0000	
			0.1			

NOP	No Operation							
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	NOP						
Operands:	None							
Operation:	No Operati	ion						
Status Affected:	None							
Encoding:	0000	0000	XXXX	XXXX	XXXX	XXXX		
Description:	No Operati	ion is perform	ied.		l			
	The 'x' bits	can take any	value.					
Words:	1							
Cycles:	1							
Example 1: NO	P ; exe	cute no ope	ration					
	Before			After				
	Instruction		Ir	nstruction				
F								
PC	00 1092		PC	00 1094				
PC SR								
_	00 1092 0000	cute no ope	PC SR	00 1094				
SR	00 1092 0000 P ; exe	cute no ope	PC SR	00 1094 0000				
SR	00 1092 0000 P ; exe Before	cute no ope	PC SR ration	00 1094 0000				
SR	00 1092 0000 P ; exe	cute no ope	PC SR ration	00 1094 0000				
SR	00 1092 0000 P ; exe Before Instruction	cute no ope	PC SR ration	00 1094 0000 After astruction				
SR [ <u>Example 2:</u> NO	00 1092 0000 P ; exer Before Instruction 00 08AE	cute no ope No Operatio	PC SR ration PC SR	00 1094 0000 After instruction 00 08B0				
SR [ Example 2: NO PC [ SR [ NOPR	00 1092 0000 P ; exer Before Instruction 00 08AE 0000	No Operatio	PC SR ration PC SR on	00 1094 0000 After nstruction 00 08B0 0000	dsPIC33F	dsPIC33		
SR [ <u>Example 2:</u> NO PC [ SR [	00 1092 0000 P ; exer Before Instruction 00 08AE		PC SR ration PC SR	00 1094 0000 After instruction 00 08B0	dsPIC33F X	dsPIC33		
SR [ <u>Example 2:</u> NO PC [ SR [ NOPR	00 1092 0000 P ; exer Before Instruction 00 08AE 0000 PIC24F	No Operatio	PC SR ration PC SR DN PIC24E	00 1094 0000 After nstruction 00 08B0 0000 dsPIC30F				
SR [ <u>Example 2:</u> Not PC [ SR [ NOPR Implemented in:	00 1092 0000 P ; exer Before Instruction 00 08AE 0000 PIC24F X	No Operation PIC24H X	PC SR ration PC SR DN PIC24E	00 1094 0000 After nstruction 00 08B0 0000 dsPIC30F				
SR [ <u>Example 2:</u> NOT PC [ SR [ NOPR Implemented in: Syntax: Operands: Operation:	00 1092 0000 P ; exer Before Instruction 00 08AE 0000 PIC24F X {label:}	No Operation PIC24H X NOPR	PC SR ration PC SR DN PIC24E	00 1094 0000 After nstruction 00 08B0 0000 dsPIC30F		dsPIC33I X		
SR <u>Example 2:</u> NOT PC SR <b>NOPR</b> Implemented in: Syntax: Operands:	00 1092 0000 P ; exer Before Instruction 00 08AE 0000 PIC24F X {label:} None	No Operation PIC24H X NOPR	PC SR ration PC SR DN PIC24E	00 1094 0000 After nstruction 00 08B0 0000 dsPIC30F				
SR [ <u>Example 2:</u> NOT PC [ SR [ NOPR Implemented in: Syntax: Operands: Operation:	00 1092 0000 P ; exer Before Instruction 00 08AE 0000 PIC24F X {label:} None No Operati	No Operation PIC24H X NOPR	PC SR ration PC SR DN PIC24E	00 1094 0000 After nstruction 00 08B0 0000 dsPIC30F				
SR [ <u>Example 2:</u> NOI PC SR [ <b>NOPR</b> Implemented in: Syntax: Operands: Operation: Status Affected:	00 1092 0000 P ; exer Before Instruction 00 08AE 0000 PIC24F X {label:} None No Operati None 1111	No Operation	PC SR ration PC SR 00 PIC24E X	00 1094 0000 After nstruction 00 08B0 0000 dsPIC30F X	X	X		
SR [ Example 2: NOT PC SR [ NOPR Implemented in: Syntax: Operands: Operation: Status Affected: Encoding:	00 1092 0000 P ; exer Before Instruction 00 08AE 0000 PIC24F X {label:} None No Operati None 1111 No Operati	No Operation PIC24H X NOPR	PC SR ration PC SR DN PIC24E X	00 1094 0000 After nstruction 00 08B0 0000 dsPIC30F X	X	X		
SR [ Example 2: NOT PC SR [ NOPR Implemented in: Syntax: Operands: Operation: Status Affected: Encoding:	00 1092 0000 P ; exer Before Instruction 00 08AE 0000 PIC24F X {label:} None No Operati None 1111 No Operati	No Operation PIC24H X NOPR ion 1111 ion is perform	PC SR ration PC SR DN PIC24E X	00 1094 0000 After nstruction 00 08B0 0000 dsPIC30F X	X	X		

Example 1: NOP	R ; exe	cute no ope	ration			
PC SR	Before Instruction 00 2430 0000		PC SR	After estruction 00 2432 0000		
Example 2: NOP	R ; exe	cute no ope	ration			
PC SR	Before Instruction 00 1466 0000		PC SR	After ostruction 00 1468 0000		
POP		Pop TOS to	f			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax: Operands:	{label:} f ∈ [0 65		f			
Operation:	(W15) – 2	-				
	(TOS) →f					
Status Affected:	None					
Encoding:	1111	1001	ffff	ffff	ffff	fff0
Description:	(TOS) word	Pointer (W15) d is written to n the lower 3	the specifie	d file register	, which may	
	The 'f' bits	select the ad	dress of the	file register.		
	Note 1:	This instruction	on operates	in Word mod	le only.	
	2:	The file regist	ter address	must be word	d-aligned.	
Words:	1					
Cycles:	1					
Example 1: POP	0x1230	; Pop TOS	to 0x1230			
Ir W15 Data 1004 Data 1230 SR	Before 15truction 1006 A401 2355 0000	W15 Data 1004 Data 1230 SR	A401 A401			

Example 2: POP	0×880	; Pop TOS	to 0x880			
In W15 Data 0880 Data 1FFE SR	Before Istruction 2000 E3E1 A090 0000	W15 Data 0880 Data 1FFE SR	A090 A090			
POP		Pop TOS to	Wd			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	POP	Wd [Wd] [Wd++] [Wd] [Wd] [++Wd] [Wd+Wb]			
Operands:	$Wd \in [W0]$ $Wb \in [W0]$					
Operation: Status Affected:	(W15) – 2 (TOS) →\ None					
Encoding:	0111	1www	w0hh	hddd	d100	1111
Description:	(TOS) wor	Pointer (W15 d is written to ed for Wd.				
	The 'h' bit	s define the o s select the de s select the de	estination Ad	dress mode.		
	Note 1: 2:	This instructi This instructi instruction (M MOV.	on is a speci	fic version of	the "MOV W	
Words:	1					
Cycles:	1					
Example 1: POP	W4	; Pop TOS	to W4			
	Before Istruction EDA8 1008 C45A 0000	W4 W15 Data 1006 SR	5 1006 5 C45A			

Example 2: POP	[++W10]	; Pre-incr ; Pop TOS				
lr W10 W15 Data 0E04 Data 1764 SR	Before Instruction 0E02 1766 E3E1 C7B5 0000		After Instruction 0E04 1764 C7B5 C7B5			
POP.D		Double Pop	TOS to Wn	d:Wnd+1		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	POP.D	Wnd			
Operands:	Wnd ∈ [W	/0, W2, W4,	W14]			
Operation:	(W15) – 2 (TOS) →V (W15) – 2 (TOS) →V	Vnd + 1 ⊥→W15				
Status Affected:	None	_				
Encoding:	1011	1110	0000	0ddd	0100	1111
Description:	Wnd:Wnd least signi	word is POPpe + 1. The mos ificant word is Pointer (W15)	t significant v stored to Wr	word is store nd. Since a d	d to Wnd + 1	., and the
	The 'd' bit	s select the ac	ldress of the	destination	register pair.	
	Note 1:	This instruction information o				
	2: 3:	Wnd must be This instruction instruction (M MOV.D.	on is a speci	fic version of	the "MOV.D	
Words:	1					
Cycles:	2					
Example 1: POP.	D W6	; Double	pop TOS t	o W6		
Ir W6 W7 W15 Data 084C Data 084E SR	Before astruction 07BB 89AE 0850 3210 7654 0000	W6 W7 W15 Data 084C Data 084E SR	7654 084C 3210 7654			

Example 2: POP.I	D WO	; Double	pop TOS to	0 W0		
In W0 W1 W15 Data 0BB8 Data 0BBA SR	Before struction 673E DD23 0BBC 791C D400 0000	W0 W1 W15 Data 0BB8 Data 0BBA SR	D400 0BB8 791C D400			
POP.S		Pop Shadov	v Registers			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	POP.S				
Operands:	None					
Operation:	POP shade	ow registers				
Status Affected:	DC, N, OV,	Z, C				
Encoding:	1111	1110	1000	0000	0000	0000
Description:	primary reg	in the shado jisters. The fo I and DC STA	llowing regis	sters are affe		
		The shadow i only be acces	ssed with PU	SH.S and PC	)P.S.	hey may
		The shadow	registers are	only one-lev	vel deep.	
Words:	1					
Cycles: Example 1: POP.S	- , - 1	o the shadow ee PUSH.S E			of shadow	s)
In W0 W1 W2 W3 SR	Before struction 07BB 03FD 9610 7249 00E0 (IPI	N N N	/2 2000 /3 3000	(IPL = 7, C =	1)	



After instruction execution, contents of shadow registers are NOT modified.

PUSH		Push f to T	os			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	PUSH	f			
Operands:	f∈ [0 65	534]				
Operation:	(f) →(TOS) (W15) + 2 →					
Status Affected:	None					
Encoding:	1111	1000	ffff	ffff	ffff	fff0
Description:	(TOS) loca	ts of the spe tion and then ister may res	the Stack P	ointer (W15)	is increment	ed by 2.
	The 'f' bits	select the ad	dress of the	file register.		
		This instruction The file regis	-		-	
Words:	1					
Cycles:	1(1)					

Note 1: In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1: PUSH	0x2004	; Push	(0x2004	) to TOS
	Before		After	
Ins	struction	1	nstructior	1
W15	0B00	W15	0B02	
Data 0B00	791C	Data 0B00	D400	
Data 2004	D400	Data 2004	D400	
SR	0000	SR	0000	
Example 2: PUSH	0×C0E	; Push (	0xC0E)	to TOS
I	Before		After	
Ins	struction	li li	nstructior	ı
W15	0920	W15	0922	
Data 0920	0000	Data 0920	67AA	
Data 0C0E	67AA	Data 2004	67AA	
SR	0000	SR	0000	

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	PUSH	Ws			
Syntax.	{Iabel.}	FUSH	[Ws]			
			[WS] [Ws++]			
			[Ws]			
			[Ws]			
			[++Ws]			
			[Ws+Wb]			
Operands:	$Ws \in [W0]$ $Wb \in [W0]$					
Operation:	(Ws) →(T (W15) + 2	,				
Status Affected:	None					
Encoding:	0111	1www	w001	1111	1ggg	SSSS
Description:		nts of Ws are tack Pointer				ation and
	The 'g' bits	s define the c s select the s s select the s	ource Addres	ss mode.		
	Note 1:	This instruct	ion operates	in Word mo	de only.	
	2:		ion is a spec MOV Ws,[W			
Words:	1					
Cycles:	1 <sup>(1)</sup>					

read-modify-write operations on non-O Special Function Regis details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

W2	; Push W2	2 to TOS
Before nstruction	ı I	After nstruction
6889	W2	6889
1566	W15	1568
0000	Data 1566	6889
0000	SR	0000
	Before nstruction 6889 1566 0000	Before           nstruction         I           6889         W2           1566         W15           0000         Data 1566

Example 2:	PUSH	[W5+W10]	;	Push	[W5+W10]	to	TOS
------------	------	----------	---	------	----------	----	-----

	Before		After		
I	nstructior	ו ו	nstruction		
W5	1200	W5	1200		
W10	0044	W10	0044		
W15	0806	W15	0808		
Data 0806	216F	Data 0806	B20A		
Data 1244	B20A	Data 1244	B20A		
SR	0000	SR	0000		

#### PUSH.D

Double Push Wns:Wns+1 to TOS

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	PUSH.D	Wns				
Operands:	Wns∈ [W	0, W2, W4	W14]				
Operation:	(Wns) →(T (W15) + 2 (Wns + 1) (W15) + 2	→W15 →(TOS)					
Status Affected:	None						
Encoding:	1011	1110	1001	1111	1000	sss0	
Description:	A double word (Wns:Wns + 1) is PUSHed to the Top-of-Stack (TOS). The least significant word (Wns) is PUSHed to the TOS first, and the most significant word (Wns + 1) is PUSHed to the TOS last. Since a double word is PUSHed, the Stack Pointer (W15) gets incremented by 4.						
	The 's' bits	s select the ac	dress of the	source regis	ster pair.		
		This instruction information o	•		-		
		Wns must be					
		This instruction (M as MOV.D.					
Words:	1						
Cycles:	2						
Example 1: PUSH	.D W6	; Push	1 W6:W7 to <sup>-</sup>	TOS			
In W6 W7 W15 Data 1240 Data 1242 SR	Before Instruction C451 3380 1240 B004 0891 0000	W6 W7 W15 Data 1240 Data 1242 SR	7 3380 5 1244 0 C451 2 3380				

Instruction Descriptions

Example 2:	PUSH.	D W10		; Push	W10:W1	1 to	T0S
		Before struction	ſ	Ir	After Instructior	ı	
	W10	80D3		W10	80D3		
	W11	4550		W11	4550		
	W15	0C08		W15	0C0C		
Data 0	)C08	79B5	Dat	ta 0C08	80D3		
Data 0	C0A	008E	Dat	a 0C0A	4550		
	SR	0000		SR	0000		
			-	_			

PUSH.S	Push Shadow Registers							
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	PUSH.S						
Operands:	None							
Operation:	PUSH sha	dow registers	6					
Status Affected:	None							
Encoding:	1111	1110	1010	0000	0000	0000		
	the C, Z, C	gisters. The f )V, N and DC The shadow only be acce The shadow	STATUS registers are ssed with PL	gister flags. e not directly JSH . S and P	accessible. <sup>-</sup> 0P <b>.</b> S.			
Words:	1							
Cycles:	1							
Example 1: PUS	H.S ; Pu	sh primary	registers	into shadow	w registers	6		
W0 W1 W2 W3 SR	1000 2000 3000	v v v	After Instruction V0 0000 V1 1000 V2 2000 V3 3000 R 0001	(C = 1)				

**Note:** After an instruction execution, contents of the shadow registers are updated.

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PWRSA	V	Enter Powe	er Saving M	ode		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	PWRSAV	#lit1			
Operands:	lit1 ∈ [0,2	L]				
Operation:	0 →WDT 0 →WDT 0 →SLEE 0 →IDLE <u>If (lit1 = 0</u> <u>Enter 5</u>	count register prescaler A co prescaler B co O (RCON<4>) EP (RCON<3> (RCON<2>) )): Sleep mode dle mode	ount ount			
Status Affected:	None					
Encoding:	1111	1110	0100	0000	0000	000k
	periphera shutdowr CPU shu periphera This instr Prescale	bde is entered. als are shutdow h. If lit1 = '1', Id ts down, but th als continue to uction resets t r Count register t System and 0 The process processor R device data If awakened and the cloc If awakened '1' and the c	vn. If an on-c le mode is e ne clock sour operate. he Watchdog rs. In additio Control regis or will exit fro eset or Watc sheet for det from Idle mo k source is a from Sleep r	hip oscillator ntered. In Idle ce remains a g Timer Cour n, the WDTO ter (RCON) a om Idle or Sle hdog Time-o ails. ode, Idle bit (1 pplied to the node, Sleep	is being use e mode, the of active and the nt register an , Sleep and I are reset. ep through a ut. See the s RCON<2>) is CPU.	d, it is also clock to the de d the dle flags o n interrupt s set to '1'
	4:	If awakened (RCON<4>)	from a Watc		ut, WDTO bi	t
Words:	1					
Cycles:	1					
Example 1:	PWRSAV #0	; Enter SL	EEP mode			
Example 2:	Before Instruction SR 0040 (I PWRSAV #1		After Instruction 0040 (I	PL = 2)		
	Before Instruction SR 0020 (I	PL = 1) SR	After Instruction	PL = 1)		

RCALL		Relative Ca	Ш					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х		Х	Х			
Syntax:	{label:}	RCALL	Expr					
Operands:		Expr may be an absolute address, label or expression. Expr is resolved by the linker to a Slit16, where Slit16 $\in$ [-32768 32767].						
Operation:		) →(TOS) →W15 >) →(TOS)	er					
Status Affected:	None							
Encoding:	0000	0111	nnnn	nnnn	nnnn	nnnn		
	<ul> <li>PUSHed onto the stack. After the return address is stacked, the sign-extended 17-bit value (2 * Slit16) is added to the contents of the Pr and the result is stored in the PC.</li> <li>The 'n' bits are a signed literal that specifies the size of the relative call program words) from (PC + 2).</li> </ul>							
	Note:	When possib	le, this instruction					
Words:	1							
Cycles:	2							
	004 006		Task1 0, W1, W2	; Cal	l _Task1			
	458 _Task1 45A	: SUB W	0, W2, W3	; _Ta	sk1 subrout	ine		
PC W15 Data 0810 Data 0812 SR	081 FFF FFF	4 0 F [ F	PC W15 Data 0810 Data 0812 SR	After nstruction 01 2458 0814 2006 0001 0000				

	0620E 06210	RCALL MOV	_Init W0, [W4++	; Call _Init ]
	•			
	07000 _Init:	CLR	W2	; _Init subroutine
0	07002			
	Before			After
	Instruction			Instruction
F	PC 00 620E		PC	00 7000
W	15 0C50		W15	0C54
Data 0C	50 FFFF		Data 0C50	6210
Data 0C	52 FFFF		Data 0C52	0000
5	SR 0000	]	SR	0000

RCALL		Relative Ca	.11				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
			Х			Х	
			_			·	
Syntax:	{label:}	RCALL	Expr				
Operands:			e address, lat inker to a Slit:			3 32767].	
Operation:	(PC<15:1> (W15) + 2 (PC<22:16 (W15) + 2 0 →SFA bit (PC) + (2 *	PC) + 2 $\rightarrow$ PC PC<15:1>) $\rightarrow$ TOS<15:1>, SFA bit $\rightarrow$ TOS<0> W15) + 2 $\rightarrow$ W15 PC<22:16>) $\rightarrow$ (TOS) W15) + 2 $\rightarrow$ W15 $\rightarrow$ $\rightarrow$ SFA bit PC) + (2 * Slit16) $\rightarrow$ PC IOP $\rightarrow$ Instruction Register					
Status Affected:	SFA	1	1	1		,	
Encoding: Description:	0000	0111	nnnn with a range o	nnnn	nnnn	nnnn	
	PUSHed o sign-extend and the res The 'n' bits	from the current PC. Before the call is made, the return address (PC + 2) PUSHed onto the stack. After the return address is stacked, the sign-extended 17-bit value (2 * Slit16) is added to the contents of the PC and the result is stored in the PC. The 'n' bits are a signed literal that specifies the size of the relative call of program words) from (PC + 2).					
	Note:		le, this instruc				
Words:	1						
Cycles:	4						
	12004 12006		_Task1 10, W1, W2	; Cal	l _Task1		
	12458 _Task1 1245A	.: SUB W	10, W2, W3	; _Ta	sk1 subrout	ine	
		04 .0 F	PC W15 Data 0810 Data 0812	After nstruction 01 2458 0814 2006 0001			
	SR 000		SR	0000			

	0620E 06210	RCALL MOV	_Init W0, [W4++	; Call _Init ]
	•			
	07000 _Init:	CLR	W2	; _Init subroutine
0	07002			
	Before			After
	Instruction			Instruction
F	PC 00 620E		PC	00 7000
W	15 0C50		W15	0C54
Data 0C	50 FFFF		Data 0C50	6210
Data 0C	52 FFFF		Data 0C52	0000
5	SR 0000	]	SR	0000

RCALL	I		Compu	ted F	Relative	Call			
Implemented in	1:	PIC24F	PIC24	Η	PIC24	E	dsPIC30F	dsPIC33F	dsPIC33E
		Х	Х				Х	Х	
Syntax:		{label:}	RCALL		Wn				
Operands:		Wn∈ [W0	W15]						
Operation:		(PC) + 2 → (PC<15:0> (W15) + 2 (PC<22:16) (W15) + 2 (PC) + (2 * NOP →Instr	) →(TOS →W15 >) →(TO →W15 (Wn)) →	S) PC	er				
Status Affected	:	None							
Encoding:		0000	000	1	0010		0000	0000	SSSS
Description: Computed, relative subroutine call specified by the working register Wn. Th range of the call is 32K program words forward or back from the current PC Before the call is made, the return address (PC + 2) is PUSHed onto the stack. After the return address is stacked, the sign-extended 17-bit value (2 (Wn)) is added to the contents of the PC and the result is stored in the PC. Register direct addressing must be used for Wn.							current PC. onto the it value (2 *		
		The 's' bits	select th	ie so	urce regi	ster.			
Words:		1							
Cycles:		2							
Example 1:	00FF80 00FF80		INC 	W2,	W3		; Dest	ination of	RCALL
	010008 010007 010000	4	RCALL MOVE	W6 W4,	[W10]		; RCAL	L with W6	
	PC W6	Before nstruction 01 000A FFC0			PC W6	Inst	After truction 00 FF8C FFC0		
V	W15	1004			W15		1008		
Data 1		98FF			ta 1004		000C		
Data 1	.006 SR	2310 0000		Dat	ta 1006 SR		0001		
					<u> </u>				

Example 2: 000 000		RCALL FF1L	W2 W0, W1	; R(	CALL with W2
		• • •			
					ation of DOAL
000		CLR	W2	; De	estination of RCALL
000	452	• • •			
	Before			After	
	Instruction			Instruction	
PC	00 0302		PC	00 0450	
W2	00A6		W2	00A6	
W15	1004		W15	1008	
Data 1004	32BB		Data 1004	0304	
Data 1006	901A		Data 1006	0000	
SR	0000		SR	0000	
		-			-

RCALL		Comput	ted F	Relative C	all		
Implemented in:	PIC24F	PIC24	Н	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
				Х			Х
Syntax:	{label:}	RCALL		Wn			
Operands:	Wn∈ [W0	W15]					
Operation:	$\begin{array}{l} (PC) + 2 \rightarrow PC \\ (PC<15:1>) \rightarrow TOS<15:1>, SFA bit \rightarrow TOS<0> \\ (W15) + 2 \rightarrow W15 \\ (PC<22:16>) \rightarrow (TOS) \\ (W15) + 2 \rightarrow W15 \\ 0 \rightarrow SFA bit \\ (PC) + (2 * (Wn)) \rightarrow PC \\ NOP \rightarrow Instruction Register \end{array}$						
Status Affected:	SFA	1				1	<b>,</b>
Encoding:	0000	0001	L	0000	0010	0000	SSSS
Description:	ption: Computed, relative subroutine call specified by the working register Wn. The range of the call is 32K program words forward or back from the current PC. Before the call is made, the return address (PC + 2) is PUSHed onto the stack. After the return address is stacked, the sign-extended 17-bit value (2 * (Wn)) is added to the contents of the PC and the result is stored in the PC. Register direct addressing must be used for Wn.						
	The 's' bits	select th	e so	urce regist	er.		
Words:	1						
Cycles:	4						
Example 1: 00FF8 00FF8		INC 	W2,	W3	; Dest	ination of	RCALL
01000	8						
01000 01000		RCALL MOVE	W6 W4,	[W10]	; RCAL	L with W6.	
	Before Instruction			I	After nstruction		
PC	01 000A			PC	00 FF8C		
W6	FFC0			W6	FFC0		
W15	1004		_	W15	1008		
Data 1004	98FF			ta 1004	000C		
Data 1006 SR	2310 0000		Dai	ta 1006 SR	0001 0000		

	302 304	RCALL FF1L	W2 W0, W1	; R(	CALL with W2
					ation of DOAL
	450 EX2:	CLR	W2	; De	estination of RCALL
000	452				
	Defere			Aftor	
	Before			After	
	Instruction			Instruction	
PC	00 0302		PC	00 0450	
W2	00A6		W2	00A6	
W15	1004		W15	1008	
Data 1004	32BB		Data 1004	0304	
Data 1006	901A		Data 1006	0000	
SR	0000		SR	0000	

REPEAT		Repeat Nex	t Instruction	n 'lit14 + 1' 1	limes	
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х		Х	Х	
Syntax:	{label:}	REPEAT	#lit14			
Operands:	lit14 ∈ [0 .	16383]				
Operation:	(lit14) $\rightarrow$ RCOUNT (PC) + 2 $\rightarrow$ PC Enable Code Looping					
Status Affected:	RA					
Encoding:	0000	1001	00kk	kkkk	kkkk	kkkk
Wordo:	<ul> <li>Repeat the instruction immediately following the REPEAT instruction (lit14 + 1) times. The repeated instruction (or target instruction) is held in the instruction register for all iterations and is only fetched once. When this instruction executes, the RCOUNT register is loaded with the repeat count value specified in the instruction. RCOUNT is decremented with each execution of the target instruction. When RCOUNT equals zero, the target instruction is executed one more time, and then normal instruction execution continues with the instruction following the target instruction. The 'k' bits are an unsigned literal that specifies the loop count.</li> <li>Special Features, Restrictions: <ol> <li>When the repeat literal is '0', REPEAT has the effect of a NOP and the RA bit is not set.</li> <li>The target REPEAT instruction cannot be: <ul> <li>an instruction that changes program flow</li> <li>a D0, DISI, LNK, MOV.D, PWRSAV, REPEAT or UNLK instruction</li> <li>a 2-word instruction</li> </ul> </li> <li>Unexpected results may occur if these target instructions are used.</li> </ol></li></ul>					
Words:	1					
Cycles: <u>Example 1:</u> 0004 0004 PC				; Execute ; Vector ( After struction	ADD 10 tin update	ies

SR

0000

0010 (RA = 1)

SR

Example 2: 0008 0008		,	cute CLR 1024 times ar the scratch space		
	Before Instruction	After Instruction			
PC	00 089E	PC	00 08A0		
RCOUNT	0000	RCOUNT	03FF		
SR	0000	SR	0010 (RA = 1)		

REPEAT	Repeat Next Instruction 'lit15 + 1' Times					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	REPEAT	#lit15			·
Operands:	lit15 ∈ [0	32767]				
Operation:	(lit15) →RC (PC) + 2 → Enable Co					
Status Affected:	RA					
Encoding:	0000	1001	0kkk	kkkk	kkkk	kkkk
Description:	<ul> <li>Repeat the instruction immediately following the REPEAT instruction (lit15 + 1) times. The repeated instruction (or target instruction) is held in the instruction register for all iterations and is only fetched once. When this instruction executes, the RCOUNT register is loaded with the repeat count value specified in the instruction. RCOUNT is decremented with each execution of the target instruction. When RCOUNT equals zero, the target instruction is executed one more time, and then normal instruction.</li> <li>The target instruction continues with the instruction following the target instruction.</li> <li>The 'k' bits are an unsigned literal that specifies the loop count.</li> <li>Special Features, Restrictions:</li> <li>When the repeat literal is '0', REPEAT has the effect of a NOP and the RA bit is not set.</li> <li>The target REPEAT instruction cannot be:         <ul> <li>an instruction that changes program flow</li> <li>a DISI, LNK, MOV.D, PWRSAV, REPEAT or UNLK instruction</li> <li>a 2-word instruction</li> <li>Unexpected results may occur if these target instructions are used.</li> </ul> </li> </ul>					
Words:	1					
Cycles: <u>Example 1:</u> 00045 00045			1, [W2++]	; Execute ; Vector u	ADD 10 tin update	nes
PC RCOUNT SR	Before Instruction 00 0452 0000 0000	R	PC COUNT SR	After struction 00 0454 0009 0010 (R	A = 1)	

Instruction Descriptions

Example 2: 0008 0008		,	cute CLR 1024 times ar the scratch space		
	Before Instruction	After Instruction			
PC	00 089E	PC	00 08A0		
RCOUNT	0000	RCOUNT	03FF		
SR	0000	SR	0010 (RA = 1)		

REPEAT		Repeat Nex		n Wn+1 Tim	es				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
	Х	Х		Х	Х				
Syntax:	{label:}	REPEAT	Wn						
Operands:	Wn∈ [W0	W15]							
Operation:	(PC) + 2 –	•) →RCOUNT ⊮PC de Looping	Г						
Status Affected:	RA								
Encoding:	0000	1001	1000	0000	0000	SSSS			
Description:	(Wn<13:0>	Repeat the instruction immediately following the REPEAT instruction (Wn<13:0>) times. The instruction to be repeated (or target instruction) is held in the instruction register for all iterations and is only fetched once.							
	lower 14 bi the target i is executed	instruction ex ts of Wn. RC nstruction. W d one more ti with the instru	OUNT is de hen RCOUN me, and the	cremented w IT equals zer n normal inst	ith each exe o, the target ruction exec	cution of instruction			
	The 's' bits	The 's' bits specify the Wn register that contains the repeat count.							
	<ol> <li>When not se</li> <li>The ta</li> <li>an in</li> <li>a DO</li> </ol>	not set.							
		a 2-word instruction							
	Unexpected results may occur if these target instructions are used.								
	Note:		-	instruction a					
Words:	1								
Cycles:	1								
	0A26 REPEAT 0A28 COM	W4 [W0++], [V		ecute COM		es			
PC W/ RCOUNT SF	4 0023 0000	R	PC W4 COUNT SR	After struction 00 0A28 0023 0023 0023 (R	A = 1)				

Example 2: 0008 0008		,	Execute TBLRD (W10+1) times Decrement (0x840)	\$	
	Before		After		
Instruction			Instruction		
PC	00 089E	PC	00 08A0		
W10	00FF	W10	00FF		
RCOUNT	0000	RCOUNT	00FF		
SR	0000	SR	0010 (RA = 1)		
RA 0000 Repeat the (Wn) times in the instr	COUNT PC ode Looping 1001 e instruction in	PIC24E X Wn 1000	0000	dsPIC33F	dsPIC33E
--	--	---	--	--	---
Wn ∈ [W0 (Wn) →RC (PC) + 2 – Enable Co RA 0000 Repeat the (Wn) times in the instr	0 W15] COUNT →PC ode Looping 1001 e instruction in	Wn 1000			<u> </u>
Wn ∈ [W0 (Wn) →RC (PC) + 2 – Enable Co RA 0000 Repeat the (Wn) times in the instr	0 W15] COUNT →PC ode Looping 1001 e instruction in	1000			
$(Wn) \rightarrow RC$ (PC) + 2 - Enable Co RA 0000 Repeat the (Wn) times in the instr	COUNT PC ode Looping 1001 e instruction in				
(PC) + 2 – Enable Co RA 0000 Repeat the (Wn) times in the instr	→PC ode Looping 1001 e instruction in				
0000 Repeat the (Wn) times in the instr	e instruction in				
Repeat the (Wn) times in the instr	e instruction in				
(Wn) times in the instr		mmodiatoly t		0000	SSSS
	s. The instruc ruction registe	tion to be rep	peated (or tai	rget instruction	on) is held
RCOUNT When RCC time, and t	instruction ex is decrement OUNT equals then normal in following the	ted with each s zero, the tar nstruction ex	n execution of rget instructio (ecution conti	f the target in on is executed	nstruction. d one more
The 's' bits	s specify the \	Wn register t	hat contains	the repeat cr	ount.
-	eatures, Res n (Wn) = 0, RE et.		ne effect of a	NOP and the	RA bit is
	et. arget REPEAT	<sup>r</sup> instruction	cannot be:		
	instruction the				
• a D inst	O, DISI, L truction	_NK, MOV.D	-	REPEAT or	ULNK
	-word instruct		torac	. truction	e ucod
-	pected results	-	-		
Note:	The Keren	ί απαταιγοι	INStruction ฉ	re interrupus	le.
1 1					
L					
REPEAT COM	W4 [W0++], [V				÷S
Before struction 00 0A26		PC W4	After Istruction 00 0A28 0023 0023		
1	1 REPEAT COM Before struction	1 1 REPEAT W4 COM [W0++], [W Before struction 00 0A26 0023 0000 R	REPEAT         W4         ; Ex           COM         [W0++], [W2++] <td; td="" ve<="">           Before         struction         In:           00 0A26         PC        </td;>	REPEAT COM       W4       ; Execute COM         COM       [W0++], [W2++] <td; completed<="" td="" vector="">         Before struction       After Instruction         00 0A26       PC       00 0A28         0002       W4       0023         0000       RCOUNT       0023</td;>	REPEAT W4     ; Execute COM (W4+1) time       COM     [W0++], [W2++]     ; Vector complement       Before     After       struction     Instruction       00 0A26     PC     00 0A28       00023     W4     0023       0000     RCOUNT     0023

Example 2: 0008 0008		,	Execute TBLRD (W10+1) time: Decrement (0x840)	s
	Before		After	
	Instruction		Instruction	
PC	00 089E	PC	00 08A0	
W10	00FF	W10	00FF	
RCOUNT	0000	RCOUNT	00FF	
SR	0000	SR	0010 (RA = 1)	

RESET		Reset				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	RESET				
Operands:	None					
Operation:	Force all re condition. 1 →SWR ( 0 →PC	gisters that a	are affected b	by a MCLR F	eset to their	Reset
Status Affected:	OA, OB, O	AB, SA, SB,	SAB, DA, DO	C, IPL<2:0>,	RA, N, OV, Z	Z, C, SFA
Encoding:	1111	1110	0000	0000	0000	0000
Description:	peripheral '0', the loca	ction provides registers will ation of the RI •), will be set	take their po ESET GOTO	wer-on value	e. The PC wil The SWR bit	l be set to
	Note:	Refer to the power-on va		-	ference mar	nual for the
Words:	1					
Cycles:	1					

Instruction Descriptions

Example 1:	00202A	RESET	; Execute sof	tware RESET	on dsPIC33F
	I	Before		After	
	Ins	struction		Instruction	
	PC	00 202A	PC	00 000	]
	W0	8901	WC	0000	
	W1	08BB	W1	0000	
	W2	B87A	W2	0000	
	W3	872F	W3	0000	
	W4	C98A	W4	0000	
	W5	AAD4	W5	0000	
	W6	981E	W6	0000	
	W7	1809	W7	0000	
	W8	C341	W8	0000	
	W9	90F4	WS	0000	
V	/10	F409	W10	0000	
V	V11	1700	W11	0000	
V	/12	1008	W12	0000	
V	/13	6556	W13	0000	
V	/14	231D	W14	0000	
V	/15	1704	W15	0800	
SPI	_IM	1800	SPLIM	0000	
TBLP	AG	007F	TBLPAG	0000	
PSVF	AG	0001	PSVPAG	0000	
CORC	ON	00F0	CORCON	0020	(SATDW = 1)
RC	ON	0000	RCON	0040	(SWR = 1)
	SR	0021	(IPL, C = 1) SR	0000	]

		Return from	interrupt			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х		Х	Х	
Syntax:	{label:}	RETFIE				
Operands:	None					
Operation:	(TOS<7>) (TOS<6:0> (W15) - 2 - (TOS<15:0	3>) →(SR<7:0 →(IPL3, COR >) →(PC<22:1	RCON<3>) 16>) :0>)			
Status Affected:	IPL<3:0>, I	RA, N, OV, Z,	, C			
Encoding:	0000	0110	0100	0000	0000	0000
Description:	loads the lo the Most S	n Interrupt Se ow byte of the significant Byte ower 16 bits o	e STATUS re e of the PC.	gister, IPL<3	3> (CORCON	l<3>) and
	2:	Restoring IPL restores the I execution wa Before RETF: must be clear	Interrupt Prio as processed IE is execute	ority Level to I. ed, the appro	the level before the le	ore the upt flag
Words:	1	Indoe			500.2.	IIup.
VV0142.	-					
Cycles:	3 (2 if exce	eption pending	3)			
Cycles: Example 1: 000A2	-		g) n from ISR			
	-		n from ISR	۸fter		
Example 1: 000A2	26 RETFIE		n from ISR	After struction		
Example 1: 000A2	26 RETFIE Before Instruction 00 0A26		n from ISR	struction 01 0230		
Example 1: 000A2	26 RETFIE Before Instruction		n from ISR	struction		
Example 1: 000A2	26 RETFIE Before Instruction 00 0A26	; Return	n from ISR	struction 01 0230		
Example 1: 000A2	26 RETFIE Before Instruction 00 0A26 0834	; Return Da	n from ISR Ins PC W15	struction 01 0230 0830		
Example 1: 000A2	26 RETFIE Before Instruction 00 0A26 0834 0230	; Return Da Da	n from ISR PC W15 tta 0830	struction 01 0230 0830 0230		
Example 1: 000A2	26 RETFIE Before Instruction 00 0A26 0834 0230 8101	; Return Da Da	PC	struction 01 0230 0830 0230 8101 0001	PL = 4, C = 1)	1
Example 1: 000A2 PC W15 Data 0830 Data 0832 CORCON	26 RETFIE Before Instruction 00 0A26 0834 0230 8101 0001 0000	; Return Da Da CC	PC	struction 01 0230 0830 0230 8101 0001	νL = 4, C = 1)	)
Example 1: 000A2 PC W15 Data 0830 Data 0832 CORCON SR	26 RETFIE Before Instruction 00 0A26 0834 0230 8101 0001 0000	; Return Da Da CC	n from ISR PC W15 tta 0830 tta 0832 DRCON SR	struction 01 0230 0830 0230 8101 0001	νL = 4, C = 1)	)
Example 1: 000A2	26 RETFIE Before Instruction 00 0A26 0834 0230 8101 0001 0000 50 RETFIE	; Return Da Da CC	n from ISR PC W15 ta 0830 ta 0832 DRCON SR n from ISR	struction 01 0230 0830 0230 8101 0001 0081 (IP	²L = 4, C = 1)	)
Example 1: 000A2	26 RETFIE Before Instruction 00 0A26 0834 0230 8101 0001 0000 50 RETFIE Before	; Return Da Da CC	n from ISR PC W15 ta 0830 ta 0832 DRCON SR n from ISR	struction 01 0230 0830 0230 8101 0001 0081 (IP	²L = 4, C = 1)	)
Example 1: 000A2	26 RETFIE Before Instruction 00 0A26 0834 0230 8101 0001 0000 50 RETFIE Before Instruction	; Return Da Da CC	n from ISR PC W15 ta 0830 DRCON SR n from ISR	struction 01 0230 0830 0230 8101 0001 0081 (IP After struction	νL = 4, C = 1)	)
Example 1: 000A2	26 RETFIE Before Instruction 00 0A26 0834 0230 8101 0001 0000 50 RETFIE Before Instruction 00 8050	; Return Da Da CC ; Return	n from ISR PC W15 ta 0830 DRCON SR n from ISR PC	struction 01 0230 0830 0230 8101 0001 0081 (IP After struction 00 7008	²L = 4, C = 1)	)

CORCON

SR

0000

0003 (Z, C = 1)

#### 5

Instruction Descriptions

CORCON

SR

0000

RETFIE		Return from	n Interrupt			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	RETFIE				
Operands:	None					
Operation:	(TOS<7>) (TOS<6:0> (W15) - 2 - (TOS<15:1 TOS<0>	<ul> <li>&gt;) →(SR&lt;7:0</li> <li>→(IPL3, COR</li> <li>→(PC&lt;22:1</li> <li>→W15</li> <li>&gt;) →(PC&lt;15:</li> </ul>	2CON<3>) .6>) :1>)			
Status Affected:	IPL<3:0>, I	RA, N, OV, Z,	C, SFA			
Encoding:	0000	0110	0100	0000	0000	0000
Description:	loads the lo the Most S	n Interrupt Se ow byte of the ignificant Byte ower 16 bits c	e STATUS re e of the PC.	egister, IPL<3	3> (CORCON	√<3>) and
	2:	Restoring IPI restores the l execution wa Before RETF must be clea	Interrupt Prid s processed IE is execut	ority Level to d. ted, the appro	the level bef	ore the upt flag
Words:	1					
Cycles:	6 (5 if exce	ption pending	g)			
Example 1: 000A2	26 RETFIE	; Return	from ISR			
	Before			After		
-	Instruction			struction		
PC	00 0A26		PC	01 0230		
W15	0834		W15	0830		
Data 0830	0230		ta 0830	0230		
Data 0832	8101		ta 0832	8101		
CORCON	0001	CC		0001		
SR	0000		SR	0081 (IF	PL = 4, C = 1	)
Example 2: 00805	50 RETFIE	; Return	from ISR			
	Before			After		
рсГ	Instruction			struction		
PC W15	00 8050		PC	00 7008		
W15	0926	D-	W15	0922		
Data 0922	7008		ta 0922	7008		
Data 0924 CORCON	0300		ta 0924 DRCON	0300		
CORCON	0000		107 1 1 11 1 I			
SR	0000		SR	0003 (Z	C = 1	

RETLW		Return with	Literal in V	Vn				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33		
	Х	Х		Х	Х			
Syntax:	{label:}	RETLW{.B}	#lit10,	Wn				
Operands:	lit10 ∈ [0 .	255] for byt 1023] for we W15]		n				
Operation:	TOS<15:8 TOS<7:0> (W15) – 2 (TOS) →(F lit10 →Wn	Wn ∈ [W0 W15] (W15) – 2 →W15 TOS<15:8> →SR<7:0> TOS<7:0> →IPL<3> : PC<22:16> (W15) – 2 →W15 (TOS) →(PC<15:0>)						
Status Affected:	None							
Encoding:	0000	0101	0Bkk	kkkk	kkkk	dddd		
	Pointer (W The 'B' bit The 'k' bits	ral is stored ir (15) is decren selects byte of s specify the v s select the de	nented by 4. or word oper value of the I	ation ('0' for iteral.				
	Note 1: 2:	The extensio rather than a denote a wor For byte ope unsigned val eral Operant operands in	word opera d operation, rations, the l ue [0:255]. S ds" for infor	tion. You may but it is not i iteral must b See <mark>Section</mark>	y use a .We required. e specified a <b>4.6 "Using 1</b>	xtension to s an L <mark>0-bit Lit-</mark>		
Words:	1							
Cycles:	3 (2 if exce	eption pending	g)					
Example 1: 00044	40 RETLW.	B #0xA, W0	; Returr	with OxA	in WO			
	Before			After				
	Instruction		In	struction				
PC	00 0440		PC	00 7006				
wo	9846		W0	980A				
W15	1988		W15	1984				
Data 1984	7006		ita 1984	7006				
Data 1986	0000	Da	ita 1986	0000				
SR	0000		SR	0000				

		<i>non</i> 200, <i>n</i> 2 , <i>n</i> 00		
	Before		After	
	Instruction		Instruction	
PC	00 050A	PC	01 7008	
W2	0993	W2	0230	
W15	1200	W15	11FC	
Data 11FC	7008	Data 11FC	7008	
Data 11FE	0001	Data 11FE	0001	
SR	0000	SR	0000	

<u>Example 2:</u> 00050A RETLW #0x230, W2 ; Return with 0x230 in W2

RETLW		Return with	n Literal in V	Nn		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
			Х			Х
Syntax:	{label:}	RETLW{.B}	#lit10,	Wn		
Operands:	-	255] for byte 1023] for we ) W15]		n		
Operation:	TOS<7:0> (W15) – 2 (TOS<15:1 TOS<0> – lit10 →Wn NOP →Ins	8> →SR<7:0> > →IPL<3>: P( →W15 1>) →(PC<15 →SFA bit	C<22:16> 5:1>)			
Status Affected:	SFA	<u> </u>	<u> </u>	· · · · · ·	· · · · · ·	
Encoding: Description:	0000	0101 m subroutine	0Bkk	kkkk	kkkk	dddd
	Pointer (W The 'B' bit The 'k' bits	ral is stored ir /15) is decrem selects byte o s specify the v s select the de	nented by 4. or word oper value of the I	ration ('0' for literal.		
	2:	denote a wor For byte ope unsigned val	a word opera rd operation, erations, the l lue [0:255]. S ids" for infor	instruction de ation. You may , but it is not i literal must be See <b>Section</b> rmation on us	y use a .We required. be specified a 4.6 "Using 1	extension to as an <b>10-bit Lit-</b>
Words:	1	operance	Jyte measu			
Cycles:		eption pending	g)			
Example 1: 00044	40 RETLW.	.B #0xA, W0	; Returr	n with OxA .	in WO	
	Before			After		
	Instruction			struction		
PC	00 0440	-	PC	00 7006		
W0	9846	-	W0	980A		
W15	1988		W15	1984		
Data 1984	7006	Da	ata 1984	7006		
		-				
Data 1986 SR	0000 0000	-	ata 1986 SR	0000		

	0000			<i>#0</i> 7230,	WZ , KC		ICH UX	200 1
			efore				fter	
		Insti	ruction			Instri	uction	_
	PC	0	0 050A		PC	0	1 7008	
	W2		0993		W2		0230	
	W15		1200		W15		11FC	
Data	11FC		7008		Data 11FC		7008	
Data	11FE		0001		Data 11FE		0001	
	SR		0000		SR		0000	]
							-	-

Example 2: 00050A RETLW #0x230, W2 ; Return with 0x230 in W2

	_	Return		1		1		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х		Х	Х			
Syntax:	{label:}	RETURN						
Operands:	None							
Operation:	(TOS) →(P (W15) – 2 (TOS) →(P	None $(W15) - 2 \rightarrow W15$ $(TOS) \rightarrow (PC<22:16>)$ $(W15) - 2 \rightarrow W15$ $(TOS) \rightarrow (PC<15:0>)$ NOP $\rightarrow$ Instruction Register						
Status Affected:	None							
Encoding:	0000	0110	0000	0000	0000	0000		
Description:		n subroutine. Ice two POPs ed by 4.						
Words:	1							
Cycles:	1 3 (2 if exce	ption pending		ubroutine				
	1 3 (2 if exce		rn from su	Ibroutine After struction 01 0004				
Cycles: Example 1: 001A	1 3 (2 if exce 96 RETURN Before Instruction		rn from su In	After struction				
Cycles: <u>Example 1:</u> 001A PC	1 3 (2 if exce 06 RETURN Before Instruction 00 1A06	; Retu	rn from su In PC	After struction 01 0004				
Cycles: <u>Example 1:</u> 001A PC W15	1 3 (2 if exce D6 RETURN Before Instruction 00 1A06 1248	; Retu Da	rn from su In PC W15	After struction 01 0004 1244				
Cycles: <u>Example 1:</u> 001A PC W15 Data 1244	1 3 (2 if exce 96 RETURN Before Instruction 00 1A06 1248 0004	; Retu Da	rn from su In PC W15 ta 1244	After struction 01 0004 1244 0004				
Cycles: <u>Example 1:</u> 001A PC W15 Data 1244 Data 1246	1 3 (2 if exce 06 RETURN Before Instruction 00 1A06 1248 0004 0001 0000	; Retu Da Da	rn from su PC W15 ta 1244 ta 1246	After struction 01 0004 1244 0004 0001 0000				
Cycles: <u>Example 1:</u> 001A PC W15 Data 1244 Data 1246 SR	1 3 (2 if exce 06 RETURN Before Instruction 00 1A06 1248 0004 0001 0000	; Retu Da Da	rn from su PC W15 ta 1244 ta 1246 SR	After struction 01 0004 1244 0004 0001 0000				
Cycles: <u>Example 1:</u> 001A PC W15 Data 1244 Data 1244 SR <u>Example 2:</u> 00544	1 3 (2 if exce before Instruction 00 1A06 1248 0004 0001 0000 04 RETURN Before Instruction	; Retu Da Da	rn from su PC W15 ta 1244 ta 1246 SR rn from su	After struction 01 0004 1244 0004 0001 0000 ubroutine After struction				
Cycles: <u>Example 1:</u> 001A PC W15 Data 1244 Data 1246 SR <u>Example 2:</u> 00540 PC	1 3 (2 if exce 36 RETURN Before Instruction 00 1A06 1248 0004 0001 0000 04 RETURN Before Instruction 00 5404	; Retu Da Da	rn from su PC W15 ta 1244 ta 1246 SR rn from su PC	After struction 01 0004 1244 0004 0001 0000 ubroutine After struction 00 0966				
Cycles: <u>Example 1:</u> 001A PC W15 Data 1244 Data 1246 SR <u>Example 2:</u> 00540 PC W15	1 3 (2 if exce 36 RETURN Before Instruction 00 1A06 1248 0004 0001 0000 94 RETURN Before Instruction 00 5404 090A	; Retu Da Da ; Retu	rn from su PC W15 ta 1244 ta 1246 SR rn from su PC W15	After struction 01 0004 1244 0004 0001 0000 ubroutine After struction 00 0966 0906				
Cycles: <u>Example 1:</u> 001A PC W15 Data 1244 Data 1244 SR <u>Example 2:</u> 0054 PC W15 Data 0906	1 3 (2 if exce Before Instruction 00 1A06 1248 0004 0001 0000 04 RETURN Before Instruction 00 5404 090A 0966	; Retu Da Da ; Retu Da	rn from su PC W15 ta 1244 ta 1246 SR rn from su PC W15 ta 0906	After struction 01 0004 1244 0004 0001 0000 ubroutine After struction 00 0966 0906 0966				
Cycles: <u>Example 1:</u> 001A PC W15 Data 1244 Data 1246 SR <u>Example 2:</u> 00540 PC W15	1 3 (2 if exce 36 RETURN Before Instruction 00 1A06 1248 0004 0001 0000 94 RETURN Before Instruction 00 5404 090A	; Retu Da Da ; Retu Da	rn from su PC W15 ta 1244 ta 1246 SR rn from su PC W15	After struction 01 0004 1244 0004 0001 0000 ubroutine After struction 00 0966 0906				

Instruction Descriptions

RETURN		Return				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
			Х			Х
Syntax:	{label:}	RETURN				
Operands:	None					
Operation:	TOS<0> →	C<22:16>) →W15 .) →(PC<15:1				
Status Affected:	SFA					
Encoding:	0000	0110	0000	0000	0000	0000
Description:		n subroutine. nce two POPs ed by 4.				
Words:	1					
Cycles:	6 (5 if exce	ption pending	g)			
Example 1: 001A	06 RETURN	; Retu	ırn from sı	ıbroutine		
	Before			After		
_	Instruction		In	struction		
PC	00 1A06		PC	01 0004		
W15	1248		W15	1244		
Data 1244	0004	Da	ita 1244	0004		
Data 1246	0001	Da	ita 1246	0001		
SR	0000		SR	0000		
Example 2: 00540	04 RETURN	; Retu	ırn from sı	ıbroutine		
	Before			After		
	Before Instruction		_In	After struction		
PC	Instruction 00 5404		PC	struction 00 0966		
W15	Instruction		PC W15	struction		
W15 Data 0906	Instruction 00 5404 090A 0966		PC W15 ta 0906	struction 00 0966 0906 0966		
W15	Instruction 00 5404 090A		PC W15	struction 00 0966 0906		

### **Section 5. Instruction Descriptions**

	Rotate Left f through Carry									
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E				
	Х	Х	Х	Х	Х	Х				
Syntax:	{label:}	RLC{.B}	f	{,WREG}						
Operands:	f∈ [08	:191]								
Operation:	<u>For byte o</u> (C) →De (f<6:0>) (f<7>) –	est<0> ) →Dest<7:1>								
	<u>For word o</u> (C) →D€	operation: est<0> >)>Dest<15::	:1>							
		<b>~</b>								
Status Affected:	N, Z, C									
Encoding:	1101	0110	1BDf	ffff	ffff	ffff				
Description:	Carry flag of the STA	e contents of th and place the ATUS Register n, and it is the	e result in the r is shifted in	e destination to the Least \$	register. The Significant bi	e Carry flag it of the				
	WREG is s	nal WREG ope specified, the the result is s	e result is stor	red in WREG						
	The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'D' bit selects the destination ('0' for f, '1' for WREG). The 'f' bits select the address of the file register.									
		rather than a denote a wor	a word operat ord operation,	instruction de tion. You may , but it is not r	y use a .Wex required.					
-		The WREG I	is set to work	king register \	<i>W</i> 0.					
Words: Cycles:	1 1									
Jycies.	T									
Example 1: RLC.	B 0x1233	; Rotat	∶e Left w/	C (0x1233)	(Byte mode	;)				
	Before		After							
_	Instruction		Instruction							
Data 1232 SR	E807 0000	Data 1232 SR		N, C = 1)						

Example 2: RLC 0x820, WREG ; Rotate Left w/ C (0x820) (Word mode) ; Store result in WREG Before After Instruction Instruction

ļ	nstruction	ו	Instruction				
WREG (W0)	5601	WRE	G (W0)	42DD			
Data 0820	216E	Dat	a 0820	216E			
SR	0001	(C = 1)	SR	0000	(C = 0)		

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	X	X	X	X	X	X
Syntax:	{label:}	RLC{.B}	Ws,	Wd		
Syman.	ງແມ່ວາວ	RLU <sub>l</sub> ,	ws, [Ws],	[Wd]		
			[vvs], [Ws++],	[Wd] [Wd++]		
			[WS++], [Ws],	[Wd++] [Wd]		
			[vvs], [++Ws],	[vvd] [++Wd]		
			[++ws], [Ws],			
			[vvəj,	[Wd]		
Operands:	$Ws \in [W0]$ $Wd \in [W0]$	) W15]				
Operation:	<u>For byte op</u> (C) →Wo	/d<0>				
	(Ws<6:0 (Ws<7>)	0>) →Wd<7:1 •) →C	_>			
	For word o	operation:				
	(C) →W0	/d<0>				
	(Ws<14: (Ws<15)	l:0>) →Wd<15 5>) →C	5:1>			
	-C-	₹				
Status Affected:	N, Z, C		_,		<del>,</del>	
Encoding:	1101	0010	1Bqq	qddd	dppp	SSSS
Description:	the Carry fl Carry flag o of Wd, and	flag and place of the STATU d it is then ove	e the result ir JS register is ⁄erwritten with	egister Ws on in the destinat s shifted into t th the Most Sig Iressing may b	tion register \ the Least Sig ignificant bit c	Wd. The gnificant bit of Ws.
	-			eration ('0' for		
	The 'q' bits	s select the de	lestination Ac	ddress mode.		Dyte <sub>j</sub> .
	The 'd' bits	s select the de	lestination re	egister.		
		s select the so s select the so				
	Note:	The extension rather than a	ion . B in the a word opera	e instruction de ation. You may	ıyusea.₩e	•
Words:	1	denoie a vvo	I'd Operation	n, but it is not	requireu.	
Words: Cycles:	1 1					
Cycles.	Ŧ					
Example 1: RLC	.C.B W0, W3		te Left w/ e the resul	C (WO) (Byt lt in W3	te mode)	
	Before		After			
W	Instruction /0 9976	W	Instruction 0 9976			
W(		W				
SF				N = 1)		
	L		L			

Instruction Descriptions

Example 2: RLC	[W2++],	, [W8]	; Post-	increme	w/ C [W2] nt W2 in [W8]	(Word	mode)
	Before			After			
I	nstructior	า	I	nstruction	า		
W2	2008		W2	200A			
W8	094E		W8	094E			
Data 094E	3689	Dat	a 094E	8082			
Data 2008	C041	Dat	a 2008	C041			
SR	0001	(C = 1)	SR	0009	(N, C = 1)		

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
·	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	RLNC{.B}	f	{,WREG}				
Operands:	f ∈ [0 8:	191]						
Operation:	(f<7>) – <u>For word c</u> (f<14:0>	→Dest<7:1> →Dest<0>	1>					
Status Affected:	N, Z	•						
Encoding:	1101	0110	0BDf	ffff	ffff	ffff		
Description:	Rotate the contents of the file register f one bit to the left and place the result in the destination register. The Most Significant bit of f is stored in the Least Significant bit of the destination, and the Carry flag is not affected.							
	The optional WREG operand determines the destination register. If WREG is specified, the result is stored in WREG. If WREG is not specified, the result is stored in the file register.							
	The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'D' bit selects the destination ('0' for WREG, '1' for file register). The 'f' bits select the address of the file register.							
	<ul> <li>Note 1: The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a . W extension to denote a word operation, but it is not required.</li> <li>2: The WREG is set to working register W0.</li> </ul>							
Words:	1							
Cycles:	1 <sup>(1)</sup>							

details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1:	RLNC.B	0x1233	;	Rotat	e Left	(0x1233)	(Byte	mode)
Data	Instru 1232 E	ore Iction 807 000	Data	l a 1233 SR	After nstruction D107 0008	n    (N = 1)		
Example 2:	RLNC 02	×820, W				(0x820) in WREG	(Word n	node)
	Bef	ore			After			
	Instru	uction		l	nstructio	n		
WREG	(W0) 5	601	WREG	G (W0)	42DC	]		
Data	0820 23	16E	Data	a 0820	216E	1		
	SR 0	001 (C	= 1)	SR	0000	(C = 0)		

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	RLNC{.B}	Ws,	Wd				
			[Ws],	[Wd]				
			[Ws++],	[Wd++]				
			[Ws],	[Wd]				
			[++Ws],	[++Wd]				
			[Ws],	[Wd]				
Operands:	Ws ∈ [W0 Wd ∈ [W0	-						
Operation:	(Ws<7> For word c	)>) →Wd<7:1 ) →Wd<0>						
		>) →Wd<0>						
Status Affected:	N, Z	1	1					
Encoding:	1101	0010	0Bqq	qddd	dppp	SSSS		
Description:	the result i stored in th	n the destina ne Least Sigr	tion register ' nificant bit of	gister Ws one Wd. The Mos Wd, and the irect address	t Significant Carry flag is	bit of Ws is not		
	The 'B' bit selects byte or word operation ('0' for byte, '1' for word). The 'q' bits select the destination Address mode. The 'd' bits select the destination register. The 'p' bits select the source Address mode. The 's' bits select the source register.							
	Note:	rather than	a word opera	instruction d ation. You ma , but it is not	y use a .We			
Words:	1							
Cycles:	1 <sup>(1)</sup>							

In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see **Note 3** in **Section 3.2.1 "Multi-Cycle Instructions"**.

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Example 1:	RLNC.B W0, W3	; Rotate Left (W0) (Byte mode) ; Store the result in W3
	Before Instruction W0 9976 W3 5879 SR 0001 (C =	After Instruction W0 9976 W3 58EC 1) SR 0009 (N, C = 1)
Example 2:	RLNC [W2++], ['	W8] ; Rotate Left [W2] (Word mode) ; Post-increment W2 ; Store result in [W8]
	Before	After
	Instruction	Instruction
	W2 2008	W2 200A
	W8 094E	W8 094E
Data	094E 3689	Data 094E 8083
Data	2008 C041	Data 2008 C041
	SR 0001 (C =	1) SR 0009 (N, C = 1)

RRC		Rotate Rig	ht f through	Carry					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	RRC{.B}	f	{,WREG}					
Operands:	f∈ [0 81	-							
Operation:	$\begin{array}{c} (C) \rightarrow De\\ (f<7:1>)\\ (f<0>) -\\ \hline\\ For word c\\ (C) \rightarrow De\\ (f<15:1> \end{array}$	For byte operation: (C) $\rightarrow$ Dest<7> (f<7:1>) $\rightarrow$ Dest<6:0> (f<0>) $\rightarrow$ C For word operation: (C) $\rightarrow$ Dest<15> (f<15:1>) $\rightarrow$ Dest<14:0> (f<0>) $\rightarrow$ C							
Status Affected:	N, Z, C								
Encoding:	1101	0111	1BDf	ffff	ffff	ffff			
	of the STA destination The option WREG is s specified, t The 'B' bit The 'D' bit	and place the ATUS Register n, and it is the nal WREG ope specified, the the result is s t selects byte o t selects the d	r is shifted in en overwritter erand detern result is stor stored in the t or word oper lestination ('6	nto the Most S n with the Lea mines the des red in WREG. file register. ration ('0' for 1 0' for WREG,	Significant bit ast Significan stination regis 5. If WREG is byte, '1' for v	t of the nt bit of Ws. ster. If s not word).			
		s select the ad		-	t - buda				
	Note 1:	rather than a	a word opera	instruction de ation. You may , but it is not r	y use a .We	•			
	2:	The WREG i	is set to worl	king register \	W0.				
Words:	1								
Cycles:	1 <sup>(1)</sup>								
read-modi	lify-write oper	24E devices, the section of the sect	n-CPU Specia	ial Function R	Registers. For				
Example 1: RRC.	.B 0x1233	; Rotat	∶e Right w/	/ C (0x1233)	) (Byte mod	le)			
Ir Data 1232 SR	Before nstruction E807 0000	Data 1232 SR							

RRC 0x820, WREG ; Rotate Right w/ C (0x820) (Word mode) Example 2: ; Store result in WREG Before After Instruction Instruction WREG (W0) 5601 WREG (W0) 90B7 Data 0820 Data 0820 216E 216E SR SR 0008 (N = 1) 0001 (C = 1)

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	RRC{.B}	Ws,	Wd					
			[Ws],	[Wd]					
			[Ws++],	[Wd++]					
			[Ws],	[Wd]					
			[++Ws],	[++Wd]					
			[Ws],	[Wd]					
Operands:		Ws ∈ [W0 W15] Wd ∈ [W0 W15]							
Operation:	For byte o (C) →W (Ws<7:1 (Ws<0> For word o	d<7> .>) →Wd<6:( ) →C	)>						
	(C) →W (Ws<15 (Ws<0>	:1>) →Wd<1	4:0>						
	▶	->C-							
Status Affected:	N, Z, C								
Encoding:	1101	0011	1Bqq	qddd	dppp	SSSS			
Description:	the Carry f Carry flag of Wd, and	lag and plac of the STATL I it is then ov	e the result i JS Register erwritten wit	egister Ws one n the destinat is shifted into h the Least S ressing may b	ion register the Most Sig ignificant bit	Vd. The nificant bit of Ws.			
	The 'q' bits The 'd' bits The 'p' bits		estination A estination re ource Addre	ss mode.		byte).			
	Note:	rather than	a word oper	instruction d ation. You ma n, but it is not	yusea.We				
Words:	1								
Cycles:	1 <sup>(1)</sup>								

**Note 1:** In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see **Note 3** in **Section 3.2.1 "Multi-Cycle Instructions**".

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Example 1: RRC	.B W0, V			•	w/ C (WO) ult in W3	(Byte	mode)
		,	00000				
	Before			After			
I	nstruction	l	I	nstructio	1		
W0	9976		W0	9976			
W3	5879		W3	58BB			
SR	0001	(C = 1)	SR	8000	(N = 1)		
			I				
	<b>EU (0</b> +	EL 10 1	<b>D</b> - 4 - 4	. Diskt			1
Example 2: RRC	[W2++],	[88]		increme	w/C[W2] nt W2	j (word	i mode)
					in [W8]		
	Before			After			
I	nstruction	l	I	nstructio	n		
W2	2008		W2	200A			
W8	094E		W8	094E			
Data 094E	3689	Data	a 094E	E020			
Data 2008	C041	Dat	a 2008	C041			
SR	0001	(C = 1)	SR	0009	(N, C = 1)		
					1		

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E				
	Х	Х	Х	Х	Х	Х				
Syntax:	{label:}	RRNC{.B}	f	{,WREG}						
Operands:	f∈ [08:	f ∈ [0 8191]								
Operation:	(f<0>) – <u>For word c</u> (f<15:1>	→Dest<6:0> →Dest<7>								
	►									
Status Affected:	N, Z									
Encoding:	1101	0111	0BDf	ffff	ffff	ffff				
Description:	Rotate the contents of the file register f one bit to the right and place the result in the destination register. The Least Significant bit of f is stored in the Most Significant bit of the destination, and the Carry flag is not affected.									
	The optional WREG operand determines the destination register. If WREG is specified, the result is stored in WREG. If WREG is not specified, the result is stored in the file register.									
	The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'D' bit selects the destination ('0' for WREG, '1' for file register). The 'f' bits select the address of the file register.									
	<ul> <li>Note 1: The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a .W extension to denote a word operation, but it is not required.</li> <li>2: The WREG is set to working register W0.</li> </ul>									
Words:	1			3 - 3 - 5 - 5 - 5	-					
Cycles:	1 <sup>(1)</sup>									

Note 1: In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1:	RRNC.B	0x1233	; Rotate	Right	(0x1233)	(Byte	mode)
	Bef			After			
	Instru	iction	Ins	truction			
Data	1232 E	807 D	ata 1232	7407			
	SR 0	000	SR	0000			
Example 2:	RRNC 0	x820, WREG	; Rotate ; Store r	•	· ,	(Word r	node)
	Bef	ore		After			
	Instru	uction	1	nstructi	on		
WREG	(W0) 5	601 V	/REG (W0)	10B7	7		
Data	0820 23	16E	Data 0820	216	Ξ		
	SR 0	001 (C = 1)	SR	000	1 (C = 1)		

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
<b>p.e</b>	X	X	X	X	X	X		
Syntax:	{label:}	RRNC{.B}	Ws,	Wd				
			[Ws],	[Wd]				
			[Ws++],	[Wd++]				
			[Ws],	[Wd]				
			[++Ws],	[++Wd]				
			[Ws],	[Wd]				
Operands:	Ws ∈ [W0 Wd ∈ [W0							
Operation:	(Ws<0>) For word o (Ws<15	1>) →Wd<6:0 •) →Wd<7>						
Status Affected:	N, Z							
Encoding:	1101	0011	0Bqq	qddd	dppp	SSSS		
Description:	place the r of Ws is stu affected. E and Wd. The 'B' bit	result in the d tored in the M Either register selects byte	destination re Aost Significa r direct or ind or word ope	egister Ws on egister Wd. Th ant bit of Wd, a direct address eration ('0' for address mode.	he Least Sigr and the Carry sing may be u word, '1' for	nificant bit y flag is not used for Ws		
	The 'd' bits select the destination register. The 'p' bits select the source Address mode. The 's' bits select the source register.							
	Note:	rather than a	a word operation	e instruction d ration. You ma n, but it is not	ay use a .W e	-		
Words:	1							

details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

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SR

0000

Example 1:	RRNC.	в W0,	W3		•	(WO) (Byte mode) sult in W3
		Before structior 9976 5879 0001	) (C = 1)	W0 W3 SR	After nstruction 9976 583B 0001	) (C = 1)
Example 2:	RRNC	[W2++	], [W8]	; Post	-increm	t [W2] (Word mode) ent W2 t in [W8]
		Before			After	
	In	structior	ı	li	nstruction	1
	W2	2008		W2	200A	
	W8	094E		W8	094E	
Data	094E	3689	Da	ta 094E	E020	
Data	2008	C041	Da	ita 2008	C041	

0008 (N = 1)

SR

Syntax:       {label}       SAC       Acc,       {#Slit4.}       Wd         Wd]       [Wd]       [Wd]       [Wd]       [Wd]         [Interpret of the status of the status of the specified accumulator, the status Affected:       None         Encoding:       1100       1100       Awww       wrrr       r hhh       dddd         Description:       Shift <sub>Slit4</sub> (Acc) (optional)       (Acc3(1:16]) -Wd       Status Affected:       None         Encoding:       1100       1100       Awww       wrrr       r hhh       dddd         Description:       Perform an optional, signed 4-bit shift of the specified accumulator, the shift across an arithmetic left shift and a positive operand indicates an arithmetic right shift.       Either shift across an arithmetic right shift.         The 'A' bit specifies the source accumulator.       The w' bits specify the offset register Wb.       The 'A' bit specifies the source accumulator pre-shift.         The 'A' bit specifies the source accumulator pre-shift.       The 'A' bit specify the destination Address mode.       The 'A' bit specify the destination accumulator pre-shift.         The 'A' bit specify the destination address mode.       The 'A' bit specify the destination address mode.       The 'A' bit specify the destination address mode.         The 'A' bit specify the destination address mode.       The 'A' bit specify the destination addres the rounded accumulator pre-shift.	Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
Wd       [Wd]         [Wd]       [Wd++]         [Wd]       [Wd]         [++Wd]       [Wd++]         [Wd]       [Wd++]         [Wd]       [Wd]         [++Wd]       [Wd + Wb]         Operation:       Shift_Slitd (-8,+7]         Wb, Wd = [W0       W15]         Operation:       Shift_Slitd(Acc) (optional)         (Acc[31:16])Wd       Status Affected:         None       Encoding:       1100       1100       Awww       wrrr       rhhh       dddd         Description:       Perform an optional, signed 4-bit shift of the specified accumulator, there store the shifted contents of ACCXH (Acc[31:16]) to Wd. The shift range is -8.7, where a negative operand indicates an arithmetic rights that and a positive operand indicates an arithmetic right shift.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator pre-shift.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator accumulator.         2 </th <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th>							
Wd       [Wd]         [Wd]       [Wd++]         [Wd]       [Wd]         [++Wd]       [Wd++]         [Wd]       [Wd++]         [Wd]       [Wd]         [++Wd]       [Wd + Wb]         Operation:       Shift_Slitd (-8,+7]         Wb, Wd = [W0       W15]         Operation:       Shift_Slitd(Acc) (optional)         (Acc[31:16])Wd       Status Affected:         None       Encoding:       1100       1100       Awww       wrrr       rhhh       dddd         Description:       Perform an optional, signed 4-bit shift of the specified accumulator, there store the shifted contents of ACCXH (Acc[31:16]) to Wd. The shift range is -8.7, where a negative operand indicates an arithmetic rights that and a positive operand indicates an arithmetic right shift.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator pre-shift.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator accumulator.         2 </td <td>O materia</td> <td>(label:)</td> <td><u> </u></td> <td><u>^</u></td> <td></td> <td>\//d</td> <td></td>	O materia	(label:)	<u> </u>	<u>^</u>		\//d	
$ \begin{array}{cccccc} & & & & & & & & & & & & & & & & $	Syntax:	{laner.}	SAC	Acc,	{#S⊪t4,∫	-	
Image: Wide-J       [Wd]         [Wd]       [++Wd]         [Wd + Wb]       Wd + Wb]         Operation:       Shiftsmd(Acc) (optional) (Acc[31:16)Wd         Status Affected:       None         Encoding:       1100       1100       Awww         Description:       Perform an optional, signed 4-bit shift of the specified accumulator, there store the shifted contents of ACCXH (Acc[31:16)) to Wd. The shift range is -8:7, where a negative operand indicates an arithmetic left shift and a positive operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd.         The 'A' bit specifies the source accumulator. The w' bits specify the offset register Wb.         The 'A' bit specifies the source accumulator pre-shift.         The 'A' bit specifies the source to word the optional accumulator accumulator accumulator contents of Acc.         2:       This instruction stores the truncated contents of Acc.         3:       if Data Write saturation is enabled (SATDW, CORCON         Words:       1 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>							
$\begin{bmatrix} [-Wd] \\ [++Wd] \\ [Wd + Wb] \end{bmatrix}$ Operands: Acc $\in [A, B]$ Slit4 $\in [-8 +7]$ Wb, Wd $\in [W0 W15]$ Operation: Shift <sub>Slit4</sub> (Acc) (optional) (Acc[31:16]) $\rightarrow$ Wd Status Affected: None Encoding: <u>1100 1100 Awww wrrr rhhh dddd</u> Description: Perform an optional, signed 4-bit shift of the specified accumulator, then store the shifted contents of ACCXH (Acc[31:16]) to Wd. The shift range is -8.7, where a negative operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd. The 'A' bit specifies the source accumulator, there 'h bits specify the offset register Wb. The 'r bits secode the optional accumulator pre-shift. The 'h' bits select the destination Address mode. The 'd' bits specify the offset register Wd. Note 1: This instruction stores the truncated contents of Acc. 2: This instruction stores the truncated contents of Acc. 3: If Data Write saturation is enabled (SATDW, CORCON-S>, = 1), the value stored to Wd is subject to saturation after the optional shift is performed. Words: 1 Cycles: 1 Example 1: SAC A, #4, W5 ; Right shift ACCA by 4 ; Store result to Ws ACCA 00 120F FF00							
$\begin{bmatrix} ++Wd \\ [Wd + Wb] \end{bmatrix}$ Operands: Acc $\in [A,B]$ Slit4 $\in [-8 +7]$ Wb, Wd $\in [W0 W15]$ Operation: Shift <sub>Slit4</sub> (Acc) (optional) (Acc[31:16]) $\rightarrow$ Wd Status Affected: None Encoding: 1100 1100 Awww wrrr rhhh dddd Description: Perform an optional, signed 4-bit shift of the specified accumulator, there store the shifted contents of ACCXH (Acc[31:16]) to Wd. The shift angle is -8:7, where a negative operand indicates an arithmetic left shift and a positive operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd. The 'A' bit specifies the source accumulator. The 'A' bit specifies the source accumulator pre-shift. The 'A' bit specifies the source accumulator pre-shift. The 'A' bit specifies the source accumulator contents. 3: If Data Write saturation is enabled (SATDW, CORCON<5>, = 1), the value stored to Wd is subject to saturation after the optional shift is performed. Words: 1 Example 1: SAC A, #4, W5 ; CORCON = 0x0010 (SATDW = 1) Before After Instruction MS B900 V/S 0120 FF00 ACCA 0120F FF00 ACCA 0120F FF00 ACCA 0120F FF00 ACCA 0120F FF00 ACCA 0120F FF00 ACCA 00120F FF00 ACCA							
$[Wd + Wb]$ Operands: Acc \in [A, B] Silit 4 \in [4 +7] Wb, Wd \in [W0 W15] Operation: Shift <sub>Silit</sub> (Acc) (optional) (Acc[31:16])Wd Status Affected: None Encoding: <u>1100 1100 Awww wrrr rhhh dddd</u> Description: Perform an optional, signed 4-bit shift of the specified accumulator, there store the shifted contents of ACCXH (Acc[31:16]) to Wd. The shift range is -8.7, where a negative operand indicates an arithmetic left shift and a positive operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd. The 'A' bit specifies the source accumulator. The 'A' bit specifies the offset register Wb. The 'r' bits specify the offset register Wd. The 'r' bits specify the offset register Wd. Note 1: This instruction does not modify the contents of Acc. 2: This instruction stores the truncated contents of Acc. 2: This instruction stores the truncated contents of Acc. 3: If Data Write saturation is enabled (SATDW, CORCON<5>, = 1), the value stored to Wd is subject to saturation after the optional shift is performed. Words: 1 Cycles: 1 Example 1: SAC A, #4, W5 ; Right shift ACCA by 4 ; Store result to W5 ; Right shift ACCA by 4 ; Store result to W5 ; CORCON = 0x0011 (SATDW = 1) Before After Instruction Mot <u>B900</u> W5 <u>0120</u> FF00 ACCA <u>0120FFF00</u> ACCA <u>0120FFF00</u> OO120 CORCON <u>0120</u> FF00							
Operands:       Acc $\in [A, B]$ Slit4 $\in [4, +7]$ Wb, Wd $\in [W0 W15]$ Operation:       Shift <sub>Slit4</sub> (Acc) (optional) (Acc[31:16])Wd         Status Affected:       None         Encoding:       1100       100       Awww       wr rr       r hhh       dddd         Description:       Perform an optional, signed 4-bit shift of the specified accumulator, there store the shifted contents of ACCXH (Acc[31:16]) to Wd. The shift range is -8.7, where a negative operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd.         The 'A' bit specifies the source accumulator. The 'A' bits specify the offset register WD. The 'A' bits specify the destination Address mode. The 'd' bits specify the destination register Wd.         Note 1:       This instruction does not modify the contents of Acc.         2:       This instruction stores the truncated contents of Acc.         2:       This instruction stores the truncated contents of Acc. The instruction SAC. R may be used to store the rounded accumulator contents.         3:       If Data Write saturation is enabled (SATDW, CORCON<5>, $= 1$ ), the value stored to Wd is subject to saturation after the optional shift is performed.         Words:       1         Example 1:       SAC A, #4, WS ; CORCON = 0x0010 (SATDW = 1)         Before       After Instruction         Most       900         Most       01207         AcccA <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>							
Slit4 $\in [-8 \dots +7]$ Wb, Wd $\in [W0 \dots W15]$ Operation:       Shift <sub>Slit4</sub> (Acc) (optional) (Acc[31:16])Wd         Status Affected:       None         Encoding:       1100       1100       Awww       wrrr       rhhh       dddd         Description:       Perform an optional, signed 4-bit shift of the specified accumulator, there is store the shifted contents of ACCxH (Acc[31:16]) to Wd. The shift range is -8.7, where a negative operand indicates an arithmetic left shift and a positive operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd.         The 'A' bit specifies the source accumulator. The 'a' bits specify the offset register Wb. The 'r' bits specify the destination Address mode. The 'a' bits specify the destination register Wd.         Note 1:       This instruction does not modify the contents of Acc.         2:       This instruction stores the truncated contents of Acc. The 'r' bits specify the destination is enabled (SATDW, CORCON<5>, = 1), the value stored to Wd is subject to saturation after the optional shift is performed.         Words:       1         Cycles:       1         Example 1:       SAC A, #4, W5 ; Store result to W5 ; CORCON = 0x0010 (SATDW = 1)         Before       After Instruction         Words:       1         Use AccA       00 120F FF00 CORCON         Quote FF00 CORCON       0010						[Wa + woj	
Wb, Wd $\in$ [WO W15]         Operation:       Shift <sub>Slit4</sub> (Acc) (optional) (Acc[31:16]) $\rightarrow$ Wd         Status Affected:       None         Encoding:       1100       1100       Awww       wrrr       rhhh       dddd         Description:       Perform an optional, signed 4-bit shift of the specified accumulator, the store the shifted contents of ACCXH (Acc[31:16]) to Wd. The shift range is -8:7, where a negative operand indicates an arithmetic left shift and a positive operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd.         The 'A' bit specifies the source accumulator. The w' bits specify the offset register Wb. The 'r' bits encode the optional accumulator pre-shift. The 'h' bits specify the destination register Wd.         Note 1:       This instruction does not modify the contents of Acc.         2:       This instruction stores the truncated contents of Acc.         2:       This instruction stores the truncated contents of Acc.         2:       This instruction stores the truncated contents of Acc.         2:       This instruction stores the truncated contents of Acc.         3:       If Data Write saturation is enabled (SATDW, CORCON         accumulator contents.       3:         3:       If Data Write saturation is enabled (SATDW, CORCON         Words:       1         Cycles:       1         Example 1:       SAC A, #4, W5	Operands:	-	-				
(Acc[31:16])Wd         Status Affected:       None         Encoding:       1100       1100       Awww       wr r r       rhhh       dddd         Description:       Perform an optional, signed 4-bit shift of the specified accumulator, there store the shifted contents of ACCxH (Acc[31:16]) to Wd. The shift range is -8.7, where a negative operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift. Either register direct or indirect addressing may be used for Wd.         The 'A' bit specifies the source accumulator.       The 'w' bits specify the offset register Wb.         The 'r' bits encode the optional accumulator pre-shift.       The 'n' bits specify the destination register Wd.         Note 1:       This instruction does not modify the contents of Acc.         2:       This instruction stores the truncated contents of Acc.         4:       The value stored to Wd is subject to saturation after the optional shift is performed.         Words:       1         Cycles:       1         Example 1:       SAC A, #4, W5         ; Right shift ACCA by 4       ; Store result to W5         ; CoRCON = 0x0010 (SATDW = 1)       Effore         After       Instruction         MVS       0120				,]			
Status Affected:       None         Encoding:       1100       1100       Awww       wrrr       rhhh       dddd         Description:       Perform an optional, signed 4-bit shift of the specified accumulator, there store the shifted contents of ACCXH (Acc[31:16]) to Wd. The shift range is -8:7, where a negative operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift and a positive operand indicates an arithmetic left shift and a positive operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator.       The 'A' bit specifies the source accumulator.         The 'A' bit specifies the source accumulator.       The 'A' bits specify the destination register Wd.         Note 1:       This instruction of acc.       2:         2:       This instruction SAC . R may be used to store the rounded accumulator contents.	Operation:			)			
Encoding:       1100       1100       Awww       wrrr       rhhh       dddd         Description:       Perform an optional, signed 4-bit shift of the specified accumulator, there store the shifted contents of ACCxH (Acc[31:16]) to Wd. The shift range is -8:7, where a negative operand indicates an arithmetic left shift and a positive operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd.         The 'A' bit specifies the source accumulator.       The 'A' bits encode the optional accumulator pre-shift.         The 'A' bits specify the destination Address mode.       The 'A' bits specify the destination register Wd.         Note 1:       This instruction does not modify the contents of Acc.         2:       This instruction stores the truncated contents of Acc.         2:       This instruction stores the truncated contents of Acc.         3:       If Data Write saturation is enabled (SATDW, CORCON         4:       Store result to W5         7:       CORCON         4:       Store result to W5	Status Affected:	• •	δ]) →Wd				
Description:       Perform an optional, signed 4-bit shift of the specified accumulator, there store the shifted contents of ACCxH (Acc[31:16]) to Wd. The shift range is -8:7, where a negative operand indicates an arithmetic left shift and a positive operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd.         The 'A' bit specifies the source accumulator. The 'w' bits specify the offset register Wb.         The 'A' bit specifies the source accumulator pre-shift.         The 'h' bits specify the destination Address mode.         The 'd' bits specify the destination register Wd.         Note 1: This instruction does not modify the contents of Acc.         2: This instruction stores the truncated contents of Acc. The instruction SAC . R may be used to store the rounded accumulator contents.         3: If Data Write saturation is enabled (SATDW, CORCON         Words:       1         Cycles:       1         Example 1:       SAC A, #4, W5         ; CoRCON = 0x0010 (SATDW = 1)         Before       After         Instruction       Instruction         Words:       1         Cycles:       1         Before       After         Instruction       Instruction         Words:       1         Cycles:       1         Corcon       0010			1100	Awww	wrrr	rhhh	dddd
store the shifted contents of ACCxH (Acc[31:16]) to Wd. The shift range is -8:7, where a negative operand indicates an arithmetic left shift and a positive operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd.         The 'A' bit specifies the source accumulator. The 'w' bits specify the offset register Wb.         The 'A' bit specifies the optional accumulator pre-shift. The 'r' bits specify the destination Address mode. The 'd' bits specify the destination register Wd.         Note 1:       This instruction does not modify the contents of Acc.         2:       This instruction stores the truncated contents of Acc. The 'd' bits specify the saturation is enabled (SATDW, CORCON<5>, = 1), the value stored to Wd is subject to saturation after the optional shift is performed.         Words:       1         Cycles:       1         Example 1:       SAC A, #4, W5 ; Right shift ACCA by 4 ; Store result to W5 ; CORCON = 0x0010 (SATDW = 1)         Before       After Instruction         W5       B900 ACCA       00 120F FF00 CORCON         0010       CORCON       0010	5						
positive operand indicates an arithmetic right shift. Either register direct or indirect addressing may be used for Wd.         The 'A' bit specifies the source accumulator.         The 'w' bits specify the offset register Wb.         The 'r' bits encode the optional accumulator pre-shift.         The 'h' bits specify the destination Address mode.         The 'd' bits specify the destination register Wd.         Note 1: This instruction does not modify the contents of Acc.         2: This instruction SAC .R may be used to store the rounded accumulator contents.         3: If Data Write saturation is enabled (SATDW, CORCON<5>, = 1), the value stored to Wd is subject to saturation after the optional shift is performed.         Words:       1         Example 1:       SAC A, #4, W5         ; Right shift ACCA by 4       ; Store result to W5         ; CORCON = 0x0010 (SATDW = 1)         Before       After         Instruction       My5         B900       ACCA         00 120F FF00       CORCON         CORCON       0010		store the s	shifted conten	nts of ACCxH	H (Acc[31:16]	]) to Wd. The	shift range
or indirect addressing may be used for Wd.         The 'A' bit specifies the source accumulator.         The 'w' bits specify the offset register Wb.         The 'r' bits encode the optional accumulator pre-shift.         The 'n' bits select the destination Address mode.         The 'd' bits specify the destination register Wd.         Note 1:       This instruction does not modify the contents of Acc.         2:       This instruction stores the truncated contents of Acc. The instruction SAC . R may be used to store the rounded accumulator contents.         3:       If Data Write saturation is enabled (SATDW, CORCON<5>, = 1), the value stored to Wd is subject to saturation after the optional shift is performed.         Words:       1         Cycles:       1         Example 1:       SAC A, #4, W5         ; Right shift ACCA by 4         ; Store result to W5         ; CORCON = 0x0010 (SATDW = 1)         Before       After         Instruction       Instruction         W5       B900       ACCA         O0 120F FF00       CORCON       0010							
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The 'w' bits specify the offset register Wb.         The 'r' bits encode the optional accumulator pre-shift.         The 'r' bits select the destination Address mode.         The 'd' bits specify the destination register Wd.         Note 1: This instruction does not modify the contents of Acc.         2: This instruction stores the truncated contents of Acc.         2: This instruction SAC. R may be used to store the rounded accumulator contents.         3: If Data Write saturation is enabled (SATDW, CORCON<5>, = 1), the value stored to Wd is subject to saturation after the optional shift is performed.         Words:       1         Cycles:       1         Example 1:       SAC A, #4, W5         ; Right shift ACCA by 4         ; Store result to W5         ; CORCON = 0x0010 (SATDW = 1)         Before       After         Instruction       Instruction         W5       B900       ACCA         00 120F FF00       ACCA       00 120F FF00         CORCON       0010       CORCON       0010			-	-			
The 'h' bits select the destination Address mode.         The 'd' bits specify the destination register Wd.         Note 1:       This instruction does not modify the contents of Acc.         2:       This instruction stores the truncated contents of Acc. The instruction SAC . R may be used to store the rounded accumulator contents.         3:       If Data Write saturation is enabled (SATDW, CORCON<5>, = 1), the value stored to Wd is subject to saturation after the optional shift is performed.         Words:       1         Cycles:       1         Example 1:       SAC A, #4, W5         ; Right shift ACCA by 4         ; Store result to W5         ; CORCON = 0x0010 (SATDW = 1)         Before       After         Instruction       Instruction         W5       B900       W5       0120         ACCA       00 120F FF00       ACCA       00 120F FF00         CORCON       0010       CORCON       0010		The 'w' bits	ts specify the	offset registe	ter Wb.		
The 'd' bits specify the destination register Wd.         Note 1: This instruction does not modify the contents of Acc.         2: This instruction stores the truncated contents of Acc. The instruction SAC.R may be used to store the rounded accumulator contents.         3: If Data Write saturation is enabled (SATDW, CORCON<5>, = 1), the value stored to Wd is subject to saturation after the optional shift is performed.         Words:       1         Cycles:       1         Example 1:       SAC A, #4, W5         ; Right shift ACCA by 4         ; Store result to W5         ; CORCON = 0x0010 (SATDW = 1)         Before       After         Instruction       Instruction         W5       B900       W5       0120         ACCA       00 120F FF00       ACCA       00 120F FF00         CORCON       0010       CORCON       0010					•		
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accumulator contents. 3: If Data Write saturation is enabled (SATDW, CORCON<5>, = 1), the value stored to Wd is subject to saturation after the optional shift is performed. Words: 1 Cycles: 1 <u>Example 1:</u> SAC A, #4, W5 ; Right shift ACCA by 4 ; Store result to W5 ; CORCON = 0x0010 (SATDW = 1) Before After Instruction Instruction W5 B900 W5 0120 ACCA 00 120F FF00 ACCA 00 120F FF00 CORCON 0010 CORCON 0010		2:					
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$= 1), the value stored to Wd is subject to saturation after the optional shift is performed.$ Words: 1 Cycles: 1 $Example 1: SAC A, #4, W5$ ; Right shift ACCA by 4 ; Store result to W5 ; CORCON = $0 \times 0010$ (SATDW = 1) Before After Instruction $W5 = B900$ W5 0120 ACCA 00 120F FF00 ACCA 00 120F FF00 CORCON 0010		3:			is enabled (S	ATDW, COR	CON<5>,
Words:1Cycles:1Example 1:SAC A, #4, W5 ; Right shift ACCA by 4 ; Store result to W5 ; CORCON = $0 \times 0010$ (SATDW = 1)BeforeAfter InstructionW5B900 0 120F FF00 ACCAW5B900 0 120F FF00 CORCONW500 120F FF00 O010CORCON0010			= 1), the valu	lue stored to	Wd is subject		
Example 1:SAC A, #4, W5 ; Right shift ACCA by 4 ; Store result to W5 ; CORCON = $0 \times 0010$ (SATDW = 1)BeforeAfter InstructionW5B900W50120ACCA00 120F FF00 O010CORCON0010	Words:	1	υριστικί ε.	10 pone	u.		
; Right shift ACCA by 4 ; Store result to W5 ; CORCON = 0x0010 (SATDW = 1) Before After Instruction Instruction W5 B900 W5 0120 ACCA 00 120F FF00 ACCA 00 120F FF00 CORCON 0010 CORCON 0010	Cycles:	1					
; Right shift ACCA by 4 ; Store result to W5 ; CORCON = $0 \times 0010$ (SATDW = 1) Before After Instruction Instruction W5 B900 W5 0120 ACCA 00 120F FF00 ACCA 00 120F FF00 CORCON 0010 CORCON 0010							
; CORCON = $0 \times 0010$ (SATDW = 1) Before After Instruction Instruction W5 B900 W5 0120 ACCA 00 120F FF00 ACCA 00 120F FF00 CORCON 0010 CORCON 0010	; R						
Instruction         Instruction           W5         B900         W5         0120           ACCA         00 120F FF00         ACCA         00 120F FF00           CORCON         0010         CORCON         0010	· ·			= 1)			
Instruction         Instruction           W5         B900         W5         0120           ACCA         00 120F FF00         ACCA         00 120F FF00           CORCON         0010         CORCON         0010		Before	٩		After		
ACCA         00 120F FF00         ACCA         00 120F FF00           CORCON         0010         CORCON         0010							
CORCON 0010 CORCON 0010	-	-		-			
SR 0000 SR 0000	CORCON SR			CORCON SR			

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Instruction Descriptions

<pre>Example 2: SAC B, #-4, [W5++] ; Left shift ACCB by 4 ; Store result to [W5], Post-increment W5 ; CORCON = 0x0010 (SATDW = 1)</pre>									
	Before		After						
	Instruction		Instruction						
W5	2000	W5	2002						
ACCB	FF C891 8F4C	ACCB	FF C891 1F4C						
Data 2000	5BBE	Data 2000	8000						
CORCON	0010	CORCON	0010						
SR	0000	SR	0000						

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
				Х	Х	Х		
Syntax:	{label:}	SAC.R	Acc,	{#Slit4,}	Wd [Wd] [Wd++] [Wd] [Wd] [++Wd] [Wd + Wb]			
Operands:	Acc ∈ [A,E Slit4 ∈ [-8 Wb ∈ [W0 Wd ∈ [W0	+7] W15]						
Operation:	Shift <sub>Slit4</sub> (A Round(Ac (Acc[31:16							
Status Affected:	None							
Encoding:	1100	1101	Awww	wrrr	rhhh	dddd		
Description:	store the r range is -8 and a posi mode (Con CORCON for Wd.	n optional, sig ounded conte 1:7, where a n tive operand nventional or <1>. Either re specifies the	ents of ACCx egative ope indicates an Convergent) gister direct	(H (Acc[31:1( rand indicate arithmetic rin ) is set by the or indirect a	6]) to Wd. Thes is an arithme ght shift. The e RND bit,	e shift tic left shift Rounding		
	The 'w' bit The 'r' bits The 'h' bits	s specify the encode the des select the des specify the d	offset registe optional accu estination Ac	er Wb. umulator pre- ldress mode				
	Note 1: 2:	,						
	3:	If Data Write $= 1$ ), the value			ATDW, CORO			
		optional shift						
Words:	1					r alter the		

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SAC.R A, #4, W5 ; Right shift ACCA by 4

; Store rounded result to W5

;  $CORCON = 0 \times 0010$  (SATDW = 1)

		After Instruction	
W5	B900	W5	0121
ACCA	00 120F FF00	ACCA	00 120F FF00
CORCON	0010	CORCON	0010
SR	0000	SR	0000

Example 2: SAC.R B, #-4, [W5++] ; Left shift ACCB by 4

; Store rounded result to [W5], Post-increment W5 ; CORCON = 0x0010 (SATDW = 1)

	Before		After
	Instruction		Instruction
W5	2000	W5	2002
ACCB	FF F891 8F4C	ACCB	FF F891 8F4C
Data 2000	5BBE	Data 2000	8919
CORCON	0010	CORCON	0010
SR	0000	SR	0000

SE		Sign-Exten	d Ws					
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	SE	Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws],	Wnd				
Operands:	$Ws \in [W0]$ Wnd $\in [W0]$	-						
Operation:	<u>If (Ws&lt;7&gt; =</u>	Wnd<15:8>						
Status Affected:	N, Z, C							
Encoding:	1111	1011	0000	0ddd	dppp	SSSS		
Description:	Sign-extend the byte in Ws and store the 16-bit result in Wnd. Either register direct or indirect addressing may be used for Ws, and register direct addressing must be used for Wnd. The C flag is set to the complement of the N flag.							
	The 'p' bits	s select the de select the so select the so	ource Addres	s mode.				
	<b>Note 1:</b> This operation converts a byte to a word, and it uses no . B or .W extension.							
		The source V address mod	Ns is address	-	e operand, so	o any		
Words:	1							
	1 <sup>(1)</sup>							

0001 (C = 1)

W4

SR

5

W4

SR

1005

008F

0000

Data 0900

SR

Example 2: SE [W2++], W12 ; Sign-extend [W2] and store to W12 ; Post-increment W2 Before After Instruction Instruction W2 0900 W2 0901 W12 1002 W12 FF8F

Data 0900

SR

008F

0008 (N = 1)

SETM		Set f or WR	EG			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	SETM{.B}	f WREG			
Operands:	f∈ [0 81	L91]				
Operation:	For word o	destination d				
Status Affected:	None					
Encoding:	1110	1111	1BDf	ffff	ffff	ffff
Description:		of the specifi WREG are se				
	The 'D' bit The 'f' bits <b>Note 1:</b>	selects byte of selects the di select the ad The extensio rather than a denote a wor The WREG i	estination ('G dress of the n . B in the in word operat d operation,	o' for WREG, file register. Instruction de ion. You may but it is not	'1' for file reg notes a byte use a .We required.	gister). operation
Words:	1			ing register		
Cycles:	1					
Example 1: SETM.B	0×891	; Set 0x89	1 (Byte mo	de)		
	Before struction 2739 0000 WREG	Data 0890 SR		e)		
	Before struction 0900 0000	WREG (W0) SR				

SETM		Set Ws				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	SETM{.B}	Wd [Wd] [Wd++] [Wd] [++Wd] [Wd]			
Operands:	Wd∈ [W0	W15]				
Operation:	For word o	Wd for byte c				
Status Affected:	None					
Encoding:	1110	1011	1Bqq	qddd	d000	0000
	The 'B' bits The 'q' bits The 'd' bits	dressing may s selects byte s select the de s select the de	or word ope estination Ad estination reg	ration ('0' foi dress mode. gister.		
	Note:	The extension rather than a denote a wo		tion. You ma	y use a .W e	
Words:	1					
Cycles:	1					
Example 1: SETM.B	W13	; Set W13	(Byte mode	)		
	Before Istruction 2739 0000 [W6]	W13 SF ; Pre-decr ; Set [W6]	2 0000 rement W6 (1	Word mode)		
	Before Istruction 1250 3CD9 0000	W6 Data 124E SF	FFFF			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
---	---	--	---	---	---	---------------------
				Х	Х	Х
Syntax:	{label:}	SFTAC	Acc,	#Slit6		
Operands:	Acc ∈ [A,B Slit6 ∈ [-16	-				
Operation:	Shift <sub>k</sub> (Acc)	→Acc				
Status Affected:	OA, OB, C	AB, SA, SB,	SAB			
Encoding:	1100	1000	A000	0000	01kk	kkkk
	shift range positive op the accum	is -16:16, wh berand indicat ulator are los	nere a negativ tes a right sh st.	sult back into t ve operand in hift. Any bits w	dicates a left	t shift and a
		selects the ac determine th		or the result. f bits to be sh	ifted.	
	Note 1: 2:	If saturation i CORCON<7 the accumula If the shift an	is enabled fo 7> or SATB, C ator is subject mount is great will be made	or the target a CORCON<6> ct to saturatio ater than 16 o to the accun	occumulator ( b), the value s n. or less than -1	stored to 16, no
Words:	1		۰ <b>۲</b>			
Cycles:	1					
; Ar: ; Ste	ore result	ight shift to ACCA 080 (SATA =				
; 00						
; 00	Before			After		
	Instructio	on	· • • • •	Instruction		
ACCA [	Instruction 00 120F F	on FF00	ACCA	Instruction 00 0001 2	OFF	
-	Instruction 00 120F F	on	ACCA CORCON SR	Instruction 00 0001 2 0		
ACCA CORCON SR Example 2: SFTAC ; Ar ; Sto	Instruction 00 120F F C B, #-10 Dithmetic lease core result	on FF00 0080 0000 eft shift A	CORCON SR	Instruction 00 0001 2 0	:0FF 0080	

5

SFTAC		Arithmetic	Shift Accun	nulator by W	'b	
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
				Х	Х	Х
Syntax:	{label:}	SFTAC	Acc,	Wb		<u> </u>
Operands:	$Acc \in [A, E]$ $Wb \in [W0]$	-				
Operation:	Shift <sub>(Wb)</sub> (A	сс) →Асс				
Status Affected:	OA, OB, O	AB, SA, SB,	SAB			
Encoding:	1100	1000	A000	0000	0000	SSSS
Description:	Arithmetic shift the 40-bit contents of the specified accumulator and store the result back into the accumulator. The Least Significant 6 bits of Wb are used to specify the shift amount. The shift range is -16:16, where a negative value indicates a left shift and a positive value indicates a right shift. Any bits which are shifted out of the accumulator are lost. The 'A' bit selects the accumulator for the source/destination.					
				e shift count re		
	2:	CORCON<7 the accumula If the shift an	> or SATB, ( ator is subject nount is great will be made	or the target a CORCON<6> ct to saturatio ater than 16 o e to the accun	e), the value n. or less than -	stored to 16, no
Words:	1		-			
Cycles:	1					
; Sto	ithmétic s ore result	hift ACCA b to ACCA 000 (satura		led)		
	Before			After		
<b>г</b>	Instructio		[	Instructio		
W0 ACCA	00 320F /	FFC	W0 ACCA	6 F 03 20FA E	FFC	
CORCON		0000	CORCON		0000	
SR		0000	SR			DAB = 1)
Example 2: SFTAG ; Ar: ; Sto	C B, W12 ithmetic s ore result	hift ACCB b	y (W12)			,
	Before			After		
Г	Instructio		,	Instruction		
W12	FF FFF1 8	000F	W12	00 FF FFFF FF	00F	
ACCB CORCON			ACCB CORCON		-E3 040	
SR		0000	SR		000	

## **Section 5. Instruction Descriptions**

JL		Shift Left f				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	SL{.B}	f	{,WREG}		
Operands:	f∈ [081	191]				
Operation:	0 →Des <u>For word c</u> (f<15>) (f<14:0> 0 →Des	$ \overrightarrow{)} \rightarrow CO $ $ \overrightarrow{)} \rightarrow Dest<7:1> $ $ st<0> $ $ operation: $ $ \overrightarrow{)} \rightarrow CO $ $ \overrightarrow{)} \rightarrow Dest<15:: $ $ st<0> $				
	[]	<b>←</b> 0				
Status Affected:	N, Z, C	. <u>.</u>	·	·	· · · · · · · · · · · · · · · · · · ·	·
Encoding: Description:	1101	0100 contents of the	0BDf	ffff	ffff	ffff
	the Least S The option WREG is s	o the Carry bit Significant bit nal WREG ope specified, the the result is st	t of the destin erand determ result is stor	nation registe mines the des red in WREG	er. stination regis	ster. If
	The 'D' bit	t selects byte o t selects the de s select the ad	lestination ('0	0' for WREG,		
	Note 1:	The extensio rather than a denote a wor	on . B in the in a word operat rd operation,	instruction de ation. You may , but it is not r	y use a . W ex required.	
	2:	The WREG is	s set to work	king register \	W0.	
Words:	1					
Cycles:	1(1)					
read-modif	ify-write oper ee <b>Note 3</b> in \$	24E devices, the stations on non <b>Section 3.2.1</b> ; Shift left	n-CPU Specia L " <b>Multi-Cycl</b>	al Function R le Instructior	Registers. For	
<u> </u>				-		
	Deforo		<b>A</b> ftor			
In Data 0908	Before nstruction 9439	Data 0908	After Instruction 8 0839			

### **16-bit MCU and DSC Programmer's Reference Manual**

; Shift left (0x1650) (Word mode) 0x1650, WREG Example 2: SL ; Store result in WREG Before After Instruction Instruction WREG (W0) 0900 WREG (W0) 80CA Data 1650 Data 1650 4065 4065 SR SR 0008 (N = 1) 0000

SL		Shift Left V	Vs			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	SL{.B}	Ws,	Wd		
			[Ws],	[Wd]		
			[Ws++],	[Wd++]		
			[Ws],	[Wd]		
			[++Ws],	[++Wd]		
			[Ws],	[Wd]		
Operands:	Ws∈ [W0 Wd∈ [W0					
Operation:	For byte o (Ws<7> (Ws<6:0 0 →Wd< For word o (Ws<15	<u>peration:</u> ) →C 0>) →Wd<7:1 :0> <u>peration:</u> >) →C :0>) →Wd<1!				
Status Affected:	C ◀ N, Z, C	-0				
Encoding:	1101	0000	0Bqq	qddd	dppp	SSSS
Description:	Shift the co the result in shifted into Least Sign	ontents of the n the destina the Carry bit	e source regi tion register t of the STAT Wd. Either re	ster Ws one I Wd. The Mos US register, a egister direct o	oit to the left t Significant and '0' is shift	and place bit of Ws is ed into the
	The 'B' bit selects byte or word operation ('0' for word, '1' for byte The 'q' bits select the destination Address mode. The 'd' bits select the destination register. The 'p' bits select the source Address mode. The 's' bits select the source register.					byte).
	Note:	rather than a	a word opera	instruction d ation. You ma 1, but it is not	yusea.We	
Words:	1					
Cycles:	1 <sup>(1)</sup>					

Note 1: In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read and read-modify-write operations on non-CPU Special Function Registers. For more details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Instruction Descriptions

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Data 1002

SR

6722

0000

ا W3 W4 SR <u>Example 2:</u> SL [۷	Before nstruction 78A9 1005 0000 /2++], [W12	W3 W4 SR ?] ; Shift ] ; Store r		(C = 1) ] (Word mode) o [W12]
	Before		After	
I	nstruction	1	nstructior	ו
W2	0900	W2	0902	
W12	1002	W12	1002	
Data 0900	800F	Data 0900	800F	

Data 1002

SR

001E

0001 (C = 1)

Example 1: SL.B W3, W4 ; Shift left W3 (Byte mode) ; Store result to W4 Before After

SL		Shift Left by	y Short Lite	ral		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	SL	Wb,	#lit4,	Wnd	
Operands:	Wb ∈ [W0 lit4 ∈ [01 Wnd ∈ [W	.5]				
Operation:		→Shift_Val hift_Val> = W Val – 1:0> = 0	_	Val:0>		
Status Affected:	N, Z					
Encoding:	1101	1101	0www	wddd	d100	kkkk
Description:	literal and s shifted out used for W The 'w' bits	e contents of store the resu of the source b and Wnd.	ult in the designed are designed at the design	tination regis lost. Direct a	ter Wnd. Any addressing n	/ bits
		select the de provide the l			nteger numb	er.
	Note:	This instruct	ion operates	in Word mo	de only.	
Words:	1					
Cycles:	1					
Example 1: SL W	2, #4, W2		eft W2 by esult to W			
W2 SR	Before nstruction 78A9 0000 3, #12, W8	W2 SR ; Shift l		12		
W3 W8 SR	Before nstruction 0912 1002 0000	W3 W8 SR	2000			

SL		Shift Left b	y Wns			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	X	Х	Х	Х	Х
Syntax:	{label:}	SL	Wb,	Wns,	Wnd	
Operands:	Wb ∈ [W0 Wns ∈ [W Wnd ∈ [W	0W15]				
Operation:	Wnd<15:S	→Shift_Val hift_Val> = W Val – 1:0> = (		t_Val:0>		
Status Affected:	N, Z					
Encoding:	1101	1101	0www	wddd	d000	SSSS
	lost. Regis The 'w' bits The 'd' bits The 's' bits <b>Note 1:</b>	register Who ter direct add s select the a select the do select the so This instructi	lressing mus ddress of the estination rep ource registe on operates	t be used for e base regist gister. r. in Word moo	<sup>.</sup> Wb, Wns ar er. de only.	id Wnd.
		If Wns is gre	ater than 15	, Wnd will be	loaded with	0×0.
Words: Cycles:	1 1					
Example 1: SL W	V0, W1, W2		eft WO by esult to w			
I W0 W1 W2 SR	Before nstruction 09A4 8903 78A9 0000	WO W1 W2 SF	8903 4D20			
Example 2: SL W	V4, W5, W6	,	eft W4 by esult to w			
I W4 W5 W6 SR	Before nstruction A409 FF01 0883 0000	W2 W5 SF	5 FF01 5 4812			

## **Section 5. Instruction Descriptions**

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
Implemented	X	X	PIC24E     X	X	X	X
	* -					
Syntax:	{label:}	SUB{.B}	f	{,WREG}		
Operands:	f∈ [0 81	191]				
Operation:	(f) – (WRE	EG) →destinat	tion designa	ted by D		
Status Affected:	DC, N, OV,	, Z, C				
Encoding: Description:	1011	0101 ne contents of	0BDf	ffff	ffff	ffff
	destination destination If WREG is	of the specified on register. The on register. If W s not specified selects byte (	e optional WI WREG is spe ed, the result	REG operan ecified, the re is stored in t	nd determine esult is stored the file regist	es the d in WREG. ter.
	The 'D' bit	selects byte of selects the d	destination ('@	0' for WREG,	G, '1' for file re	
	Note 1:	rather than a denote a wor	on . B in the i a word operat ord operation,	instruction de tion. You may , but it is not	denotes a byt ay use a .W e t required.	
Words:	<b>2</b> :	The wkr∟€.	is set to work	KING เยษาอเอา	WU.	
Words: Cycles:	1 1 <b>(1)</b>					
read-modify details, see <u>Example 1:</u> SUB.B 0	fy-write oper e <b>Note 3</b> in <b>S</b> 0×1FFF ; Before	24E devices,t rations on nor <b>Section 3.2.1</b> Sub. WREG Store resu	n-CPU Specia 1 "Multi-Cycl from (0x1F ult to 0x1F After	ial Function F cle Instructio FFF) (Byte FFF	Registers. Fo ons".	
In: WREG (W0) Data 1FFE SR	nstruction 7804 9439 0000 0xA04, WRE	G ; Sub.	Instruction V0) 7804 FE 9039	(C = 1) (0×A04) (W	√ord mode)	
	Before nstruction 6234 4523 0000	WREG (M Data 0A	404 4523	]		

SUB		Subtract Li	teral from W	/n		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	SUB{.B}	#lit10,	Wn		
Operands:		255] for byt 1023] for we W15]		1		
Operation:	(Wn) – lit1	0 →Wn				
Status Affected:	DC, N, OV	, Z, C				
Encoding:	1011	0001	0Bkk	kkkk	kkkk	dddd
Description:	Subtract the 10-bit unsigned literal operand from the contents of the working register Wn, and store the result back in the working register Wn. Register direct addressing must be used for Wn.					
	The 'k' bits The 'd' bits Note 1: 2:	selects byte of specify the list select the ad The extension rather than a denote a wor For byte ope unsigned val eral Operant operands in the	teral operand ddress of the n . B in the in word operat d operation, rations, the li ue [0:255]. S ds" for inform	d. working reg nstruction de ion. You may but it is not r iteral must be see <b>Section</b>	notes a byte v use a . W ex required. e specified a: 4.6 "Using 1	xtension to s an <b>0-bit Lit-</b>
Words:	1					
Cycles:	1					
Example 1: SUB.B	#0x23, W0		0x23 from result to	WO (Byte mo WO	ode)	
Ir W0 SR <u>Example 2:</u> SUB	Before nstruction 7804 0000 #0×108, W	W0 SR 4 ; Sub.	0008 (N	W4 (Word n	node)	
lr W4 SR	Before Instruction 6234 0000	W4 SR		:=1)		

SUB						
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	SUB{.B}	Wb,	#lit5,	Wd	
					[Wd]	
					[Wd++]	
					[Wd]	
					[++Wd]	
					[Wd]	
Operands:	Wb ∈ [W0 lit5 ∈ [0 Wd ∈ [W0	31]				
Operation:	(Wb) – lit5	-				
Status Affected:	DC, N, OV	, Z, C				
Encoding:	0101	0www	wBqq	qddd	d11k	kkkk
	direct addr		be used for		on register W <sup>r</sup> direct or ind	
	The 'B' bit The 'q' bits The 'd' bits	selects byte s select the d s select the d	or word open lestination Ac	ddress mode gister.	word, '1' for	
	Note:	rather than	a word opera		lenotes a byt ay use a .W e required.	
Words:	1		·			
Cycles:	1					
Example 1: SUB.B	W4, #0x10	, ,	ub. 0x10 fr tore result	rom W4 (Byt) to W5	e mode)	
	Before struction		After Instruction			
W4	1782	W				
W5	7804	W				
SR	0000	SF	۲ 0005 (۵	OV, C = 1)		
Example 2: SUB	W0, #0×8,			from WO (W sult to [W2 rement W2		
	Before Instruction F230 2004 A557	Wi Wi	2 2006			
	455/	Data 2004	4 F228			

Implemented in: Syntax:	PIC24F X {label:}	PIC24H X	PIC24E	dsPIC30F	dsPIC33F	
Syntax:		Х			USPICSSE	dsPIC33
Syntax:	{label:}		Х	Х	Х	Х
		SUB{.B}	Wb,	Ws,	Wd	
				[Ws],	[Wd]	
				[Ws++],	[Wd++]	
				[Ws],	[Wd]	
				[++Ws],	[++Wd]	
				[Ws],	[Wd]	
Operands:	Wb ∈ [W0 Ws ∈ [W0 Wd ∈ [W0	W15]				
Operation:	(Wb) – (W	s) →Wd				
Status Affected:	DC, N, OV	, Z, C				
Encoding:	0101	0www	wBqq	qddd	dppp	SSSS
			iace the resi	ilt in the dest		
	Register di indirect ad The 'w' bits The 'B' bit The 'q' bits	rect address dressing may s select the a selects byte s select the de	ng must be be used for ddress of the or word oper estination Ac	used for Wb. Ws and Wd e base regist ration ('0' for ddress mode.	ination regist Either regist er. word, '1' for l	ter Wd. er direct o
	Register di indirect ad The 'w' bits The 'B' bit The 'q' bits The 'd' bits The 'p' bits	irect addressi dressing may s select the a selects byte	ng must be be used for ddress of the or word oper estination Ac estination re ource Addres	used for Wb. Ws and Wd base regist ration ('0' for ddress mode. gister. ss mode.	ination regist Either regist er. word, '1' for l	ter Wd. er direct o
	Register di indirect ad The 'w' bits The 'B' bit The 'q' bits The 'd' bits The 'p' bits	rect addressi dressing may s select the a selects byte s select the de select the de select the so select the so The extension rather than a	ng must be be used for ddress of the or word oper estination Ac estination re- burce Addres burce register on . B in the a word opera	used for Wb. Ws and Wd e base regist ration ('0' for ddress mode. gister. ss mode. rr. instruction d	ination regist Either regist er. word, '1' for l enotes a byt y use a . W e	ter Wd. er direct o byte). e operatio
Words:	Register di indirect ad The 'w' bits The 'B' bit The 'q' bits The 'q' bits The 'p' bits The 's' bits	rect addressi dressing may s select the a selects byte s select the de select the de select the so select the so The extension rather than a	ng must be be used for ddress of the or word oper estination Ac estination re- burce Addres burce register on . B in the a word opera	used for Wb. Ws and Wd e base regist ration ('0' for ddress mode. gister. ss mode. rr. instruction d ation. You ma	ination regist Either regist er. word, '1' for l enotes a byt y use a . W e	er direct o byte). e operatio

	Before		After	
I	nstructior	n I	nstructior	า
W0	1732	W0	17EE	
W1	7844	W1	7844	
SR	0000	SR	0108	(DC, N = 1)

Example 2: SUB	W7, [W8++],		Sub. [W8] from W7 (Word mode) Store result to [W9] Post-increment W8 Post-increment W9
	Before		After
I	nstruction	l.	nstruction
W7	2450	W7	2450
W8	1808	W8	180A
W9	2020	W9	2022
Data 1808	92E4	Data 1808	92E4
Data 2020	A557	Data 2020	916C
SR	0000	SR	010C (DC, N, OV = 1)

SUB		Subtract A	ccumulator	S				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
				Х	Х	Х		
Syntax:	{label:}	SUB	Acc					
Operands:	$Acc \in [A,B]$							
Operation:	ACCA – A	If (Acc = A): ACCA – ACCB →ACCA Else: ACCB – ACCA →ACCB						
Status Affected:	OA, OB, OA	AB, SA, SB,	SAB					
Encoding:	1100	1011	A011	0000	0000	0000		
Description:		store the re		ified accumu o Acc. This ir				
	The 'A' bit s	pecifies the	destination	accumulator.				
Words:	1							
Cycles:	1							
Example 1: SUB	; St	ore the re	B from ACC sult to AC 0000 (no sa	CA				
	Before			After				
	Instruction			Instructio				
ACCA ACCB	76 120F 0 23 F312 B		ACCA ACCB	52 1EFC 4 23 F312 E				
CORCON		000	CORCON		0000			
SR		0000	SR			)B = 1)		
Example 2: SUB	; St	ore the re	A from ACC sult to AC 040 (SATB	СВ				
	Before			After				
_	Instruction	۱ <u> </u>	_	Instructior				
ACCA	FF 9022 2E		ACCA	FF 9022 2E				
ACCB	00 2456 8F		ACCB	00 7FFF FF				
CORCON					040			
SR	0	000	SR	1	400 (SB, S	AB = 1)		

SUBB	Subtract WREG and Carry bit from f								
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	SUBB{.B}	f	{,WREG}					
Operands:	f∈ [0 82	191]							
Operation:	(f) – (WRE	$(\overline{C}) \to de$	estination de	signated by	D				
Status Affected:	DC, N, OV	, Z, C							
Encoding:	1011	0101	1BDf	ffff	ffff	ffff			
	register an WREG op specified, t	Subtract the contents of the default working register WREG and the Borrow flag (Carry flag inverse, $\overline{C}$ ) from the contents of the specified file register and place the result in the destination register. The optional WREG operand determines the destination register. If WREG is specified, the result is stored in WREG. If WREG is not specified, the result is stored in the file register							
	The 'D' bit	selects byte of selects the d select the ad	estination ('(	9' for WREG	, '1' for file re				
	<ul> <li>The 'f' bits select the address of the file register.</li> <li>Note 1: The extension . B in the instruction denotes a byte operat rather than a word operation. You may use a .W extensior denote a word operation, but it is not required.</li> <li>2: The WREG is set to working register W0.</li> <li>3: The Z flag is "sticky" for ADDC, CPB, SUBB and SUBBR.</li> </ul>								
		These instru							
Words:	1								
Cycles:	1(1)								
read-modi	fy-write oper e <b>Note 3</b> in 9 0x1FFF ;	24E devices, t rations on nor <b>Section 3.2.1</b> Sub. WREG Store resu	-CPU Speci "Multi-Cyc and C from	al Function F le Instructio	Registers. Fo ns".	r more			
	Before		After						
	struction		Instruction						
WREG (W0) Data 1FFE	7804	WREG (W0) Data 1FFE							
SR	9439 0000	Dala IFFE		DC, C = 1)					
L	xA04, WREG	; Sub. WR		rom (0xA04	) (Word mo	de)			
Ir WREG (W0) Data 0A04 SR	Before astruction 6234 6235 0000	WREG (W0) Data 0A04 SR	6235	C = 1)					

SUBB	Subtract Wn from Literal with Borrow							
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	SUBB{.B}	#lit10,	Wn				
Operands:	lit10 ∈ [0	lit10 $\in$ [0 255] for byte operation lit10 $\in$ [0 1023] for word operation Wn $\in$ [W0 W15]						
Operation:	(Wn) – lit10	0 – ( <del>C</del> ) →Wn						
Status Affected:	DC, N, OV	, Z, C						
Encoding:	1011	0001	1Bkk	kkkk	kkkk	dddd		
Description:	Subtract the unsigned 10-bit literal operand and th flag inverse, C) from the contents of the working r the result back in the working register Wn. Register must be used for Wn.					and store		
	The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'k' bits specify the literal operand. The 'd' bits select the address of the working register.							
		The extensio rather than a denote a wor	word operat	ion. You may	usea.we			
		For byte ope unsigned val eral Operano operands in I	ue [0:255]. S <mark>ds</mark> " for infori	See Section	4.6 "Using 1	.0-bit Lit-		
		The Z flag is These instrue			SUBB and S	SUBBR.		
Words:	1							
Cycles:	1							
Example 1: SUBB.B	#0x23, W	,	0x23 and e result t	⊂ from WO ( o WO	(Byte mode)	1		
	Before struction 7804 0000 #0x108, W	WC SR 4 ; Sub.	0108 (	DC,N=1) C from W4 ( W4	(Word mode)	1		
	Before struction 6234 0001 (C	W4		2 = 1)				

	BB Subtract Short Literal from Wb with Borrow						
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х	Х	Х	х	Х	
Syntax:	{label:}	SUBB{.B}	Wb,	#lit5,	Wd		
					[Wd]		
					[Wd++]		
					[Wd]		
					[++Wd]		
					[Wd]		
Operands:	Wb ∈ [W0 lit5 ∈ [0 Wd ∈ [W0	31]					
Operation:		$-(\overline{C}) \rightarrow Wd$					
Status Affected:	DC, N, OV	, Z, C					
Encoding:	0101	1www	wBqq	qddd	d11k	kkkk	
	result in th used for W	e destination	register Wd	f the base reç . Register dir r indirect addı	ect addressir	d place the	
	result in th used for W Wd. The 'W' bits The 'B' bit The 'q' bits The 'd' bits	e destination 'b. Either regi s select the a selects byte s select the d s select the d	register Wd ster direct or ddress of th or word oper estination Ad estination re	f the base reg . Register dir r indirect addu e base regist ration ('0' for ddress mode. gister.	yister Wb and ect addressir ressing may I er. word, '1' for	d place the ng must be be used fo byte).	
	result in th used for W Wd. The 'w' bits The 'B' bit The 'q' bits The 'd' bits The 'k' bits	e destination 'b. Either regi s select the a selects byte s select the d s select the d s provide the	register Wd ster direct of ddress of th or word oper estination Ad estination re literal operat	f the base reg . Register dir r indirect addr e base regist ration ('0' for ddress mode. gister. nd, a five-bit i	yister Wb and ect addressir ressing may l er. word, '1' for nteger numb	d place the ng must be be used fo byte). er.	
	result in th used for W Wd. The 'w' bits The 'B' bit The 'q' bits The 'd' bits The 'k' bits	e destination 'b. Either regins s select the a selects byte s select the d s select the d provide the The extension rather than a	register Wd ster direct or ddress of th or word ope estination Ad estination re literal operation . B in the word operation	f the base reg . Register dir r indirect add e base regist ration ('0' for ddress mode. gister. nd, a five-bit i instruction de tion. You may	yister Wb and ect addressin ressing may l er. word, '1' for nteger numb enotes a byte y use a . W ex	d place the ng must be be used fo byte). er. operation	
	result in th used for W Wd. The 'w' bits The 'B' bit The 'q' bits The 'd' bits <b>Note 1:</b>	e destination 'b. Either regi s select the a selects byte s select the d s select the d s provide the The extension rather than a denote a wo The Z flag is	register Wd ster direct of ddress of th or word oper estination Ad estination re literal operation . B in the i a word operation "sticky" for	f the base reg . Register dir r indirect add e base regist ration ('0' for ddress mode. gister. nd, a five-bit i instruction de tion. You may , but it is not ADDC, CPB	yister Wb and ect addressin ressing may l er. word, '1' for nteger numb enotes a byte y use a . W ex required.	d place the ng must be be used fo byte). er. operation ktension to	
Words:	result in th used for W Wd. The 'w' bits The 'B' bit The 'q' bits The 'd' bits <b>Note 1:</b>	e destination 'b. Either regi s select the a selects byte s select the d s select the d s provide the The extension rather than a denote a wo	register Wd ster direct of ddress of th or word oper estination Ad estination re literal operation . B in the i a word operation "sticky" for	f the base reg . Register dir r indirect add e base regist ration ('0' for ddress mode. gister. nd, a five-bit i instruction de tion. You may , but it is not ADDC, CPB	yister Wb and ect addressin ressing may l er. word, '1' for nteger numb enotes a byte y use a . W ex required.	d place the ng must be be used fo byte). er. operation ktension to	
Words: Cycles:	result in th used for W Wd. The 'w' bits The 'B' bit The 'q' bits The 'd' bits The 'k' bits <b>Note 1</b> : 2:	e destination 'b. Either regi s select the a selects byte s select the d s select the d s provide the The extension rather than a denote a wo The Z flag is	register Wd ster direct of ddress of th or word oper estination Ad estination re literal operation . B in the i a word operation "sticky" for	f the base reg . Register dir r indirect add e base regist ration ('0' for ddress mode. gister. nd, a five-bit i instruction de tion. You may , but it is not ADDC, CPB	yister Wb and ect addressin ressing may l er. word, '1' for nteger numb enotes a byte y use a . W ex required.	d place the ng must be be used fo byte). er. operation ktension to	
Cycles:	result in th used for W Wd. The 'w' bits The 'B' bit The 'q' bits The 'd' bits <b>Note 1:</b> 2:	e destination 'b. Either regi s select the a selects byte s select the d s select the d provide the The extension rather than a denote a wo The Z flag is These instru	register Wd ster direct of ddress of th or word oper estination Ac estination re literal operation . B in the word operation "sticky" for ctions can o	f the base reg . Register dir r indirect add e base regist ration ('0' for ddress mode. gister. nd, a five-bit i instruction de tion. You may , but it is not i ADDC, CPB nly clear Z.	yister Wb and ect addressin ressing may l er. word, '1' for nteger numb enotes a byte y use a . W ex required. , SUBB and	d place the ng must be be used for byte). er. operation ktension to SUBBR.	
Cycles: Example 1: SUBB.	result in th used for W Wd. The 'w' bits The 'B' bit The 'q' bits The 'd' bits The 'k' bits Note 1: 2: 1 1 8 W4, #0x1 Before	e destination 'b. Either regi s select the a selects byte s select the d s select the d provide the The extension rather than a denote a wo The Z flag is These instru	register Wd ster direct of ddress of th or word oper estination Ad estination re literal operation . B in the is word operation "sticky" for ctions can o	f the base reg . Register dir r indirect add e base regist ration ('0' for ddress mode. gister. nd, a five-bit i instruction de tion. You may , but it is not i ADDC, CPB nly clear Z.	yister Wb and ect addressin ressing may l er. word, '1' for nteger numb enotes a byte y use a . W ex required. , SUBB and	d place the ng must be be used fo byte). er. operation ktension to SUBBR.	
Cycles: Example 1: SUBB.	result in th used for W Wd. The 'w' bits The 'B' bit The 'q' bits The 'd' bits The 'k' bits Note 1: 2: 1 1 B W4, #0x1 Before Instruction	e destination b. Either reginners s select the anselects byte s select the d s select the select s s s select the select s s s s s s s s s s s s s s s s s s s	register Wd ster direct of ddress of th or word oper estination Ad estination re literal operation "B in the word operation "sticky" for ctions can o ub. 0x10 ar core result After Instruction	f the base reg . Register dir r indirect add e base regist ration ('0' for ddress mode. gister. nd, a five-bit i instruction de tion. You may , but it is not i ADDC, CPB nly clear Z.	yister Wb and ect addressin ressing may l er. word, '1' for nteger numb enotes a byte y use a . W ex required. , SUBB and	d place the ng must be be used fo byte). er. operation ktension to SUBBR.	
Cycles: Example 1: SUBB.	result in th used for W Wd. The 'w' bits The 'B' bit The 'q' bits The 'd' bits The 'k' bits Note 1: 2: 1 1 B W4, #0x1 Before Instruction 1782	e destination 'b. Either regi s select the a selects byte s select the d s select the d provide the The extension rather than a denote a wo The Z flag is These instru	register Wd ster direct of ddress of th or word oper estination Ad estination re literal operation "B in the in word operation "sticky" for ctions can o ub. 0x10 ar core result After Instruction 4 1782	f the base reg . Register dir r indirect add e base regist ration ('0' for ddress mode. gister. nd, a five-bit i instruction de tion. You may , but it is not i ADDC, CPB nly clear Z.	yister Wb and ect addressin ressing may l er. word, '1' for nteger numb enotes a byte y use a . W ex required. , SUBB and	d place the ng must be be used fo byte). er. operation ktension to SUBBR.	

### 5

<u>Example 2:</u> SUBB W0, #0x8, [W2++] ; Sub. 0x8 and  $\overline{C}$  from W0 (Word mode) ; Store result to [W2] ; Post-increment W2 Before After Instruction Instruction 0009 0009 W0 W0 W2 2004 W2 2006 Data 2004 A557 Data 2004 0000 SR 0002 (Z = 1) SR 0103 (DC, Z, C = 1)

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33		
	X	X	X	X	X	Х		
Suptay:	{label:}	SUBB{.B}	Wb,	Ws,	Wd			
Syntax:	{iabel.}	3000[.0]	VVD,					
				[Ws],	[Wd]			
				[Ws++],	[Wd++]			
				[Ws],	[Wd]			
				[++Ws],	[++Wd]			
				[Ws],	[Wd]			
Operands:	Wb ∈ [W0 Ws ∈ [W0 Wd ∈ [W0	W15]						
Operation:	(Wb) – (W	s) – $(\overline{C}) \rightarrow W$	d					
Status Affected:	DC, N, OV							
Encoding:	0101	1www	wBqq	qddd	dppp	SSSS		
Description:	Subtract th	ne contents o		register Ws a		w flag		
	The 'B' bit The 'q' bits The 'd' bits The 'p' bits	The 'w' bits select the address of the base register. The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'q' bits select the destination Address mode. The 'd' bits select the destination register. The 'p' bits select the source Address mode.						
		The 's' bits select the source register.						
	Note 1:	Note 1: The extension . B in the instruction denotes a byte operat rather than a word operation. You may use a .W extensio denote a word operation, but it is not required.						
	2:							
Words:	1			<b>)</b>				
Cycles:	1 <sup>(1)</sup>							
read-mo	33E and PIC2 dify-write oper see <b>Note 3</b> in \$ B W0, W1,	ations on no Section 3.2.1	n-CPU Speci L "Multi-Cyc	al Function R	egisters. For ns".			
		; Sto	re result t	to W0				
	Before		After Instruction					
W	Instruction	W						
W		W						

Example 2: SUBB	W7,[W8++],[W9	; Sto ; Pos		
	Before		After	
I	nstruction	l	nstructior	1
W7	2450	W7	2450	
W8	1808	W8	180A	
W9	2022	W9	2024	
Data 1808	92E4	Data 1808	92E4	
Data 2022	A557	Data 2022	916B	
SR	0000	SR	010C	(DC, N, OV = 1)

SUBBR		Subtract f f	rom WREG	with Borro	w		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	SUBBR{.B}	f	{,WREG}			
Operands:	f∈ [0 81	.91]					
Operation:	(WREG) –	$(f) - (\overline{C}) \rightarrow de$	stination de	signated by I	D		
Status Affected:	DC, N, OV	Z, C					
Encoding:	1011	1101	1BDf	ffff	ffff	ffff	
	<ul> <li>in the destination register. The optional WREG operand determines the destination register. If WREG is specified, the result is stored in WREG If WREG is not specified, the result is stored in the file register.</li> <li>The 'B' bit selects byte or word operation ('0' for word, '1' for byte).</li> <li>The 'D' bit selects the destination ('0' for WREG, '1' for file register).</li> <li>The 'f' bits select the address of the file register.</li> <li>Note 1: The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a .W extension to denote a word operation, but it is not required.</li> <li>2: The WREG is set to working register W0.</li> <li>3: The Z flag is "sticky" for ADDC, CPB, SUBB and SUBBR.</li> </ul>						
Words:		These instruc			0022 0.10		
Cycles:	1(1)						
read-modii details, se	fy-write oper e <b>Note 3</b> in <b>S</b>	4E devices, th ations on non Section 3.2.1 Sub. (0x80 Store resu	-CPU Specia "Multi-Cycl 3) and C f	al Function R e Instruction	egisters. For ns".		
WREG (W0) Data 0802 SR	Before Instruction 7804 9439 0002 (Z = 0xA04, WRE	G ; Sub. (0	02 6F39 SR 0000	C from WRE	G (Word mo	de)	
lr WREG (W0) Data 0A04 SR	Before astruction 6234 6235 0000	WREG (W Data 0A S	·				

# 5

<u>\_\_\_\_</u>

SUBBR		Subtract W	b from Shoi	rt Literal wit	h Borrow			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	х	х	Х		
Syntax:	{label:}	SUBBR{.B}	Wb,	#lit5,	Wd [Wd] [Wd++] [Wd] [++Wd] [Wd]			
Operands:	Wb ∈ [W0 lit5 ∈ [0 Wd ∈ [W0	31]						
Operation:	lit5 – (Wb)	$-(\overline{C}) \rightarrow Wd$						
Status Affected:	DC, N, OV	, Z, C						
Encoding:	0001	1www	wBqq	qddd	d11k	kkkk		
Description:	Subtract the contents of the base register Wb and the Borrow flag (Car flag inverse, C) from the 5-bit unsigned literal and place the result in th destination register Wd. Register direct addressing must be used for W Register direct or indirect addressing must be used for Wd.							
	<ul> <li>Register direct or indirect addressing must be used for Wd.</li> <li>The 'w' bits select the address of the base register.</li> <li>The 'B' bit selects byte or word operation ('0' for word, '1' for byte).</li> <li>The 'q' bits select the destination Address mode.</li> <li>The 'd' bits select the destination register.</li> <li>The 'k' bits provide the literal operand, a five-bit integer number.</li> <li>Note 1: The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a .W extension to</li> </ul>							
	2:	denote a wor The Z flag is	d operation,	but it is not	required.			
	Ζ.	These instruc			SUBB and S	JUDDK.		
Words:	1							
Cycles:	1							
Example 1: SUBBR.	B W0, #0x	10, W1 ; Su ; St	b. WO and ore result		0 (Byte moc	le)		
I W0	Before nstruction F310	WO	After Instruction F310					

W1

SR

7800

0103 (DC, Z, C = 1)

W1

SR

786A

0003 (Z, C = 1)

<u>ampie 2:</u>	SURRK	WU, #U)	<8, [W2++]	; St	ore res	ult to [W2] ement W2	(word	ШС
		Before			After			
	l	nstruction	1	I	nstructior	ו		
	W0	0009		W0	0009			
	W2	2004		W2	2006			
Dat	ta 2004	A557	Data 2	2004	FFFE			
	SR	0020	(Z = 1)	SR	0108	(DC, N = 1)		

<u>Example 2:</u> SUBBR W0, #0x8, [W2++]; Sub. W0 and  $\overline{C}$  from 0x8 (Word mode)

SUBBR	Subtract Wb from Ws with Borrow							
Implemented in:	PIC24F PIC24H PIC24E			dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	SUBBR{.B}	Wb,	Ws,	Wd			
				[Ws], [Ws++],	[Wd] [Wd++]			
				[WS],	[Wd]			
				[++Ws],	[++Wd]			
				[Ws],	[Wd]			
Operands:	$Wb \in [W0]$ $Ws \in [W0]$ $Wd \in [W0]$	W15] W15]						
Operation:	. , .	$(\overline{C}) \rightarrow Wd$						
Status Affected:	DC, N, OV	1	L D a a	addd	doop			
Encoding: Description:	0001	1www e contents of	wBqq	qddd	dppp	SSSS		
	flag inverse, C) from the contents of the source register Ws and place the result in the destination register Wd. Register direct addressing must be used for Wb. Register direct or indirect addressing may be used for Ws and Wd.							
	The 'B' bit The 'q' bits The 'd' bits The 'p' bits	selects byte o	or word oper estination Ac estination re- ource Addres	ess mode.				
	<b>Note 1:</b> The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a .W extension to denote a word operation, but it is not required.							
	2:	The Z flag is These instruc	"sticky" for A	ADDC, CPB,	•	SUBBR.		
Words:	1							
Cycles:	1 <sup>(1)</sup>							
read-modi	fy-write oper	4E devices, tl ations on non Section 3.2.1	-CPU Speci	al Function R	egisters. For			
Example 1: SUBBR.	B W0, W1,		. W0 and <del>C</del> re result	from W1 (E to W0	Byte mode)			
lr Wo	Before Instruction	W0	After Instruction					

W1

SR

7844

0001 (C = 1)

W1

SR

7844

0000

Example 2: SUBBR	W7,[W8+	+],[W9++]	; Sto ; Pos			(Word mode)	
	Before			After			
I	nstructior	۱	I	nstructior	ו		
W7	2450		W7	2450			
W8	1808		W8	180A			
W9	2022		W9	2024			
Data 1808	92E4	Data	1808	92E4			
Data 2022	A557	Data	2022	6E93			
SR	0000		SR	0005	(OV, C = 1)		

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SUBR		Subtract f	from WREG	; 			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33	
	Х	Х	Х	Х	Х	Х	
Syntax:	{label:}	SUBR{.B}	f	{,WREG}			
Operands:	f∈ [082	191]					
Operation:	(WREG) –	(WREG) – (f) $\rightarrow$ destination designated by D					
Status Affected:	DC, N, OV	′, Z, C					
Encoding:	1011	1101	0BDf	ffff	ffff	ffff	
	destinatior destinatior If WREG is	Subtract the contents of the specified file register from the contents of the default working register WREG, and place the result in the destination register. The optional WREG operand determines the destination register. If WREG is specified, the result is stored in WREG If WREG is not specified, the result is stored in the file register					
	The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'D' bit selects the destination ('0' for WREG, '1' for file register). The 'f' bits select the address of the file register.						
	<b>Note 1:</b> The extension . B in the instruction denotes a byte operation rather than a word operation. You may use a W extension denote a word operation, but it is not required.						
	2:	The WREG i	-		-		
Words:	1						
Cycles:	1 <sup>(1)</sup>						
read-mod	lify-write oper ee <b>Note 3</b> in 9		n-CPU Speci . " <mark>Multi-Cyc</mark>	al Function F le Instructio	Registers. Fo ns".		
I WREG (W0) Data 1FFE SR Example 2: SUBR	9439	WREG (WO Data 1FFE SF G ; Sub. ( ; Store	7039 0000 (0xA04) fro	om WREG (Wo	rd mode)		
<u> </u>		,	Tesuit to	WILLO			

SUBR		Subtract W				
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	SUBR{.B}	Wb,	#lit5	Wd	
					[Wd]	
					[Wd++]	
					[Wd]	
					[++Wd]	
					[Wd]	
Operands:	Wb∈ [W0					
	lit5 ∈ [0 Wd ∈ [W0					
Operation:	lit5 – (Wb)	-				
Status Affected:	DC, N, OV					
Encoding:	0001	, 2, C 0www	wBqq	qddd	d11k	kkkk
Description:		-		gister Wb fro		
Description.				in the destin		
		irect address dressing ma		used for Wb. r Wd	Either regist	er direct c
			-	e base regist	er.	
	The 'B' bit	selects byte	or word ope	ration ('0' for	word, '1' for	byte).
				ddress mode		
		s select the d		gister. nd, a five-bit	integer numb	oer.
	Note:	The extensi	on . B in the	instruction d ation. You ma	enotes a byt	e operatic
				i, but it is not		
Words:	1					
Cycles:	1					
Example 1: SUBR.B	W0, #0×1		ub. W0 from tore result		e mode)	
	Before		After			
wo	struction F310	W	Instruction 0 F310			
W0 W1	786A	W				
SR	0000	SI		DC, Z, C = 1)	)	
Example 2: SUBR		[W2++] ·		rom 0x8 (Wo		
	,,	;	Store res	ult to [W2]	i a modoj	
		;	Post-incre	ement W2		
Ir	Before struction		After Instruction			
wo	0009	W				
W2	2004	W				
Data 2004	A557	Data 200	4 FFFF			

Instruction Descriptions

 $\ensuremath{\textcircled{}^\circ}$  2005-2011 Microchip Technology Inc.

SUBR		Subtract W	/b from Ws			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
			•	4		
Syntax:	{label:}	SUBR{.B}	Wb,	Ws,	Wd	
				[Ws],	[Wd]	
				[Ws++],	[Wd++]	
				[Ws],	[Wd]	
				[++Ws],	[++Wd]	
				[Ws],	[Wd]	
Operands:	Wb ∈ [W0 Ws ∈ [W0 Wd ∈ [W0	W15]				
Operation:	(Ws) – (Wl	bW← (c				
Status Affected:	DC, N, OV	, Z, C		1	1	<b>-</b>
Encoding:	0001	0www	wBqq	qddd	dppp	SSSS
Description:	Subtract the contents of the base register Wb from the contents of the source register Ws and place the result in the destination register Wd. Register direct addressing must be used for Wb. Either register direct or indirect addressing may be used for Ws and Wd. The 'w' bits select the address of the base register. The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'q' bits select the destination Address mode. The 'd' bits select the destination register. The 'p' bits select the source Address mode.					ister Wd. er direct or
	The 's' bits	select the se	ource registe	er.		
	Note:	rather than	a word opera	instruction d ation. You ma , but it is not	ay use a .We	
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-modif	iy-write oper e <b>Note 3</b> in <b>\$</b>	ations on nor Section 3.2.1	n-CPU Speci L "Multi-Cyc	le count does al Function R le Instruction /1 (Byte more o W0	egisters. For ns".	
In W0 W1 SR	Before Istruction 1732 7844 0000	y star W( W) SF	After Instruction 0 1712 1 7844			

Example 2: SUBR	W7, [W8++],	;	Store r Post-in	from [W8] (Word mode) esult to [W9] crement W8 crement W9
	Before		After	
I	nstruction	li li	nstruction	า
W7	2450	W7	2450	
W8	1808	W8	180A	
W9	2022	W9	2024	
Data 1808	92E4	Data 1808	92E4	
Data 2022	A557	Data 2022	6E94	
SR	0000	SR	0005	(OV, C = 1)

SWAP		Byte or Nit	ble Swap V	Vn		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	SWAP{.B}	Wn			
Operands:	Wn∈ [W0	W15]				
Operation:	(Wn)<7:4 For word of	For byte operation: $(Wn)<7:4> \leftrightarrow (Wn)<3:0>$ For word operation: $(Wn)<15:8> \leftrightarrow (Wn)<7:0>$				
Status Affected:	None					
Encoding:	1111	1101	1B00	0000	0000	SSSS
	Wn is unch The 'B' bit s	Byte of Wn a anged. Regis selects byte o select the ac	ster direct ac	ddressing mu ation ('0' for	ust be used t word, '1' for	for Wn.
	Note:	select the ac The extension rather than a denote a wo	on . B in the a word opera	instruction c tion. You ma	lenotes a by ay use a .W	
Words:	1		ia operation	,	. oqui ou	
Cycles:	1					
Example 1: SWAP.B	W0 ; M	Nibble swap	(W0)			
	Before struction AB87 0000	WC SR	_			
Example 2: SWAP	W0 ; E	Byte swap (	WO)			
In W0 SR	Before struction 8095 0000	W0 SR				

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	TBLRDH{.B}	[Ws],	Wd		
			[Ws++],	[Wd]		
			[Ws],	[Wd++]		
			[++Ws],	[Wd]		
			[Ws],	[++Wd]		
				[Wd]		
Operands:	Ws ∈ [W0 . Wd ∈ [W0	-				
Operation:	For byte operation: $\frac{\text{If (LSB(Ws) = 1)}}{0 \rightarrow Wd}$ Else Program Mem [(TBLPAG),(Ws)] <23:16> $\rightarrow Wd$					
	For word of	<u>peration:</u> Mem [(TBLPA				
Status Affected:	None					
Encoding:	1011	1010	1Bqq	qddd	dppp	SSSS
Description:	Read the contents of the most significant word of program memory and store it to the destination register Wd. The target word address of program memory is formed by concatenating the 8-bit Table Pointer register, TBLPAG<7:0>, with the effective address specified by Ws. Indirect addressing must be used for Ws, and either register direct or indirect addressing may be used for Wd.					
	register (du memory by	de, zero is sto le to non-existe te (PM<23:16> e Least Signifi	ent program ( >) at the spec	memory) and cified progran	the third pro	ogram
	In Byte mode, the source address depends on the contents of Ws. If Ws not word-aligned, zero is stored to the destination register (due to non-existent program memory). If Ws is word-aligned, the third program memory byte (PM<23:16>) at the specified program memory address is stored to the destination register.					
	The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'q' bits select the destination Address mode. The 'd' bits select the destination register. The 'p' bits select the source Address mode. The 's' bits select the source register.					
		The extension than a word n word move, bu	nove. You m	ay use a .W	-	
Words:	1					
Cycles:	2 (PIC24F,	PIC24H, dsPI	C30F, dsPIC	33F)		
,						

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#### **16-bit MCU and DSC Programmer's Reference Manual**



Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E	
Шрепенса	X	РІС24Н Х	X X	X	X	X	
Syntax:	{label:}	TBLRDL{.B}		Wd			
Symax.	{lauci.j	ΙΟΓΝοτίνοι	[wsj, [Ws++],	Wd [Wd]			
			[WS++], [WS],	[vva] [Wd++]			
			[vvs], [++Ws],	[Wd++] [Wd]			
			[++vvs], [Ws],	[vvu] [++Wd]			
			[vv3],	[++vvd] [Wd]			
Operands:	Ws∈ [W0	-					
	Wd ∈ [W0	-					
Operation:	For byte op If (LSB(\	<u>peration:</u> Ws) = 1)					
	Progra	ram Mem [(TBL	LPAG),(Ws)]	<15:8> →Wd	I		
	Else Progra	ram Mem [(TBL	י האסין (۱۸/א)]	p///۲ <sup>–</sup> ۲۰۰۲			
	Progra <u>For word o</u>		_PAG),(vv3)]	:U →vvu			
	Program	n Mem [(TBLP/	AG),(Ws)] <1	.5:0> →Wd			
Status Affected:	None						
Encoding:	1011	1010	0Bqq	ddd	dppp	SSSS	
Description:	store it to th memory is TBLPAG<7 addressing	contents of the the destination formed by con 7:0>, with the e g must be used g may be used	register Wd. ncatenating th effective addr d for Ws, and	The target we he 8-bit Table ress specified	ord address of Pointer regis I by Ws. Indir	of program ster, rect	
	In Word mode, the lower 2 bytes of program memory are stored to the destination register. In Byte mode, the source address depends on the contents of Ws. If Ws is not word-aligned, the second byte of the program memory word (PM<15:7>) is stored to the destination register. If Ws is word-aligned, the first byte of the program memory word (PM<7:0>) is stored to the destination register.						
	The 'B' hit				ord mode '1'		
	The 'q' bits The 'd' bits The 'p' bits	selects byte or s select the des s select the des s select the sou s select the sou	stination Add stination regis urce Address	lress mode. ster. s mode.	olu moue, ±	for byte).	
	The 'q' bits The 'd' bits The 'p' bits	s select the des s select the des s select the sou	stination Add stination regis urce Address urce register. n .B in the in move. You n	Iress mode. ster. s mode. nstruction den nay use a .w	iotes a byte n	move rathe	
Words:	The 'q' bits The 'd' bits The 'p' bits The 's' bits	s select the des s select the des s select the sou s select the sou The extension than a word of	stination Add stination regis urce Address urce register. n .B in the in move. You n	Iress mode. ster. s mode. nstruction den nay use a .w	iotes a byte n	move rathe	
Words: Cycles:	The 'q' bits The 'd' bits The 'p' bits The 's' bits <b>Note:</b> 1	s select the des s select the des s select the sou s select the sou The extension than a word of	stination Add stination regis urce Address urce register. n . B in the in move. You n but it is not rea	Iress mode. ster. s mode. nstruction den may use a .w quired.	iotes a byte n	move rathe	

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## **16-bit MCU and DSC Programmer's Reference Manual**

Example 1: TBLF	RDL.B [W0++	], W1 ; Read PM ( ; Store to ; Post-incr	W1	) (Byte mode)
	Before		After	
	Instruction		Instruction	
W0	0813	W0	0814	
W1	0F71	W1	0F20	
Data 0F70	0944	Data 0F70	EF44	
Program 01 0812	EF 2042	Program 01 0812	EF 2042	
TBLPAG	0001	TBLPAG	0001	
SR	0000	SR	0000	
Example 2: TBLF	RDL [W6],	[W8++] ; Read PM	I (TBLPAG:[W	(luord mode)
		; Store t	· -	6]) (word mode)
	Before	; Store t	o`W8	6j) (word mode)
	Before Instruction	; Store t	co`W8 Icrement W8	6j) (word mode)
W6	Instruction 3406	; Store t	o w8 ocrement W8 After Instruction 3406	6j) (word mode)
W6 W8	Instruction	; Store t ; Post-in	o W8 Icrement W8 After Instruction	6j) (word mode)
	Instruction 3406 1202 658B	; Store t ; Post-in W6	o w8 ocrement W8 After Instruction 3406	6j) (word mode)
W8	Instruction 3406 1202	; Store t ; Post-in W6 W8	After Instruction 3406 1204	6j) (word mode)
W8 Data 1202	Instruction 3406 1202 658B	; Store t ; Post-in W6 W8 Data 1202	After Instruction 3406 1204 2E40	6j) (word mode)

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	TBLWTH{.B}	Ws,	[Wd]		
	-		[Ws],	[Wd++]		
			[Ws++],	[Wd]		
			[Ws],	[++Wd]		
			[++Ws],	[Wd]		
			[Ws],	L		
Operands:	Ws∈ [W0 Wd∈ [W0					
Operation:	For byte op If (LSB(V NOP <u>Else</u>	peration: Wd) = 1)				
	- (Ws) For word o	→Program Mer <u>operation:</u> :0> →Program N	. ,			
Status Affected:	None					
Encoding:	1011	1011	1Bqq	qddd	dppp	SSSS
Description:	word of pro memory is TBLPAG<7	contents of the v ogram memory. formed by con 7:0>, with the e ldressing may b Vd.	v. The destinancatenating the	ation word add he 8-bit Table ress specified	dress of prog Pointer regis by Wd. Eithe	gram ster, er direct or
	upper byte a Wd that i	gram memory is e of program me is word-aligned a Wd that is not	emory (PM<2 d in Byte mod	23:16>). This r de or Word mo	may be perfor	rmed using node is
	The 'q' bits The 'd' bits The 'p' bits	selects byte or s select the des s select the des s select the sou s select the sou	stination Addr stination regis urce Address	lress mode. ster. s mode.	ərd, '1' for byt	:e).
		The extension than a word me move, but it is	nove. You may	ay use a . W ext		
Words:	1					
Cycles:	2 <sup>(1)</sup>					
		IC24E devices, perations on no	on-CPU Spec		Registers. For	

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Example 1: TBLV	√TH.B [W0++]			e mode) TBLPAG:[W1])	
	Before		After		
	Instruction	Instruction			
W0	0812	W0	0814		
W1	0F70	W1	0F70		
Data 0812	0944	Data 0812	EF44		
Program 01 0F70	EF 2042	Program 01 0F70	44 2042		
TBLPAG	0001	TBLPAG	0001		
SR	0000	SR	0000		

**Note:** Only the Program Latch is written to. The contents of program memory are not updated until the Flash memory is programmed using the procedure described in the specific device family reference manual.

Example 2:	TBLWTH	W6, [W8++]	; Write W6 (Word mode) ; to PM Latch High (TBLPAG:[W8]) ; Post-increment W8
			,



**Note:** Only the Program Latch is written to. The contents of program memory are not updated until the Flash memory is programmed using the procedure described in the specific device family reference manual.
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	TBLWTL{.B}	Ws,	[Wd]		
- J · · · ·	U -	••	[Ws],	[Wd++]		
			[₩3], [Ws++],	[Wd]		
			[Ws],	[++Wd]		
			[++Ws],	[Wd]		
			[Ws],	ι.		
Operands:	Ws ∈ [W0 . Wd ∈ [W0 .					
Operation:	<u>For byte op</u> If (LSB(V (Ws) –		m [(TBLPAG	•) (Wd)] <15:8	5	
	Else	-				
	– (Ws) – <u>For word op</u>	→Program Mer	m [(TBLPAG)	),(Wd)] <7:0>		
		p <u>eration:</u> Program Mem [	آ(TBLPAG),(۱	Wd)] <15:0>		
Status Affected:	None		X			
Encoding:	1011	1011	0Bqq	qddd	dppp	SSSS
	memory is 1 TBLPAG<7	ogram memory. formed by con 7:0>, with the e dressing may b /d.	ncatenating th	he 8-bit Table ress specified	Pointer regis I by Wd. Eithe	ster, er direct or
	In Word mo Byte mode, If Wd is not memory (Pl	ode, Ws is stor , the Least Sig t word-aligned, PM<15:8>). If W iemory (PM<7:	gnificant bit of I, Ws is storec Vd is word-ali	f Wd determin d to the secon	nes the destin nd byte of pro	nation byte. ogram
	The 'B' bit s The 'q' bits The 'd' bits The 'p' bits	selects byte or select the des select the des select the sou select the sou	r word operati stination Addr stination regis urce Address	lress mode. ster. s mode.	rd, '1' for byt	e).
	Note:	The extension than a word m move, but it is	n . B in the in nove. You may	nstruction den ay use a .Wext		
Words:	1					
Cycles:	2 <sup>(1)</sup>					
		IC24E devices,			es not apply to Registers. For	

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Instruction Descriptions

Example 1: TBL	√TL.B ₩0, [W		(Byte mode) ch Low (TBLPAG:[W1]) ement W1
	Before Instruction		After Instruction
W0	6628	W0	6628
W1	1225	W1	1226
Program 00 1224	78 0080	Program 01 1224	78 2880
TBLPAG	0000	TBLPAG	0000
SR	0000	SR	0000

**Note:** Only the Program Latch is written to. The contents of program memory are not updated until the Flash memory is programmed using the procedure described in the specific device family reference manual.

Example 2: TBLV	VTL [W6],		] (Word ch Low (TBL ement W8	,
	Before		After	
	Instruction		Instruction	
W6	1600	W6	1600	
W8	7208	W8	7208	
Data 1600	0130	Data 1600	0130	
Program 01 7208	09 0002	Program 01 7208	09 0130	
TBLPAG	0001	TBLPAG	0001	
SR	0000	SR	0000	

**Note:** Only the Program Latch is written to. The contents of program memory are not updated until the Flash memory is programmed using the procedure described in the specific device family reference manual.

# **Section 5. Instruction Descriptions**

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х		Х	Х	
Syntax:	{label:}	ULNK				
Operands:	None					
Operation:	W14 →W1 (W15) – 2 (TOS) →W	→W15				
Status Affected:	None					
Encoding:	1111	1010	1000	0000	0000	0000
Description:	sequence. (W15) equ	ction de-alloo The Stack Fi al to the Frar e Frame Poir	rame is de-a ne Pointer (	llocated by s	etting the Sta	ack Pointer
Words:	1					
Cycles:	1					
	Before struction 2002 20A2 2000 0000	W14 W15 Data 2000 SF	5 2000 2000			
Example 2: ULNK	; Unlink	the stack	frame			
	Before struction 0802 0812 0800 0000	W14 W15 Data 0800 SF	5 0800 0 0800			

ULNK		De-allocate	Stack Fran	ne		
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33
			Х			Х
Syntax:	{label:}	ULNK				
Operands:	None					
Operation:	W14 →W1 (W15) – 2 (TOS) →W 0 →SFA bi	→W15 /14				
Status Affected:	SFA					
Encoding:	1111	1010	1000	0000	0000	0000
Description:	sequence. (W15) equ	iction de-alloc The Stack Fr ial to the Fran e Frame Poin	ame is de-a ne Pointer (\	llocated by s	etting the Sta	ack Pointe
Words:	1					
Cycles:	1					
Example 1: ULNK	; Unlin	< the stack	frame			
E	Before		After			
	struction		Instruction			
W14	2002	W14				
W15	20A2	W15				
Data 2000 SR	2000 0000	Data 2000 SR				
51	0000	30	0000			
Example 2: ULNK	; Unlin	< the stack	frame			
	Before		After			
	struction		Instruction			
W14		W14				
	0812	W15				
W15	0800	0000 eted				
Data 0800	0800	Data 0800 SR				
	0800 0000	Data 0800 SR				
Data 0800						

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	XOR{.B}	f	{,WREG}				
Operands:	f∈ [0 81	191]						
Operation:	(f).XOR.(V	VREG) →dest	tination desi	gnated by D				
Status Affected:	N, Z			5				
Encoding:	1011	0110	1BDf	ffff	ffff	ffff		
	register an WREG ope specified, t result is ste	rking register nd place the re erand determ the result is st ored in the file	esult in the d nines the des tored in WR e register.	destination regis stination regis EG. If WREG	gister. The o ster. If WREG is not speci	ptional 5 is fied, the		
	The 'B' bit selects byte or word operation ('0' for word, '1' for byte). The 'D' bit selects the destination ('0' for WREG, '1' for file register). The 'f' bits select the address of the file register.							
	Note 1:	The extensio rather than a denote a wor	on . B in the i word opera rd operation,	instruction de tion. You may , but it is not r	y use a . W e required.	•		
	2:	The WREG I	s set to won	king register \	<i>N</i> 0.			
Words:	1							
Cycles:	1(1)							
		24E devices, t		le count ແບ <del>ບ</del> ອ	S not apply to	- d and		
details, se <u>Example 1:</u> XOR.B	ee Note 3 in 8 0x1FFF Before nstruction 7804 9439	Section 3.2.1 ; XOR (0x1 ; Store re	. <b>"Multi-Cycl</b> LFFF) and we esult to 0× After Instruction ) 7804 = 9039	WREG (Byte n <1FFF	egisters. For ns".			
details, se <u>Example 1:</u> XOR.B WREG (W0) Data 1FFE	ee Note 3 in 8 0x1FFF Before nstruction 7804 9439	Section 3.2.1 ; XOR (0x1 ; Store re WREG (W0) Data 1FFE SR REG ; XOR (	LFFF) and we sult to 0x After Instruction ) 7804 9039 R 0008 (N	<b>le Instruction</b> WREG (Byte m <1FFF N = 1) d WREG (Word	registers. For ns". mode)			

XOR		Exclusive C	OR Literal and Wn						
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E			
	Х	Х	Х	Х	Х	Х			
Syntax:	{label:}	XOR{.B}	#lit10,	Wn					
Operands:	lit10 $\in$ [0 255] for byte operation lit10 $\in$ [0 1023] for word operation Wn $\in$ [W0 W15]								
Operation:	lit10.XOR.	(Wn) →Wn							
Status Affected:	N, Z								
Encoding:	1011	0010	1Bkk	kkkk	kkkk	dddd			
Description:	Compute the logical exclusive OR operation of the unsigned 10-bit lit operand and the contents of the working register Wn and store the re back in the working register Wn. Register direct addressing must be used for Wn.								
	The 'k' bits The 'd' bits <b>Note 1:</b>	selects byte of specify the li select the ac The extensio rather than a denote a wor For byte oper unsigned value operands in F	teral operan Idress of the n . B in the in word operat d operation, rations, the I ue [0:255]. S ds" for inform	d. working reg nstruction de ion. You may but it is not r iteral must be see <b>Section</b>	ister. notes a byte / use a . W ex required. e specified as 4.6 "Using 1	operation ktension to s an <b>0-bit Lit-</b>			
Words:	1								
Cycles:	1								
Example 1: XOR.B	#0x23, W0	,	0x23 and W e result t	0 (Byte moc o W0	le)				
W0 SR	Before nstruction 7804 0000 #0x108, W4	W0 SR ; XOR	0000	W4 (Word mc o W4	ode )				
lr W4 SR	Before nstruction 6134 0000	W4 SR							

Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E
	Х	Х	Х	Х	Х	Х
Syntax:	{label:}	XOR{.B}	Wb,	#lit5,	Wd	
					[Wd]	
					[Wd++] [Wd]	
					[Wd] [++Wd]	
					[Wd]	
					[]	
Operands:	Wb ∈ [W0 lit5 ∈ [0 Wd ∈ [W0	. 31]				
Operation:	(Wb).XOF	≀.lit5 →Wd				
Status Affected:	N, Z					
Encoding:	0110	1www	wBqq	qddd	d11k	kkkk
Description:	register W the destin	the logical exe /b and the uns ation register r register dire	signed 5-bit li Wd. Registe	iteral operand r direct addre	d and place t essing must b	he result in be used for
	The 'B' bit The 'q' bit The 'd' bit	ts select the a selects byte s select the de s select the de s provide the	or word oper estination Ac estination reg	ation ('0' for Idress mode. gister.	word, '1' for	
	Note:	rather than a	a word opera	instruction d tion. You ma , but it is not	yusea.We	
Words:	1			,	1090	
Cycles:	1					
Example 1: X0	)R.B W4, #0)	×14, W5		und 0x14 (By esult to W5	yte mode)	
	Before		After			
W	Instruction 4 C822	١٨	Instruction /4 C822	1		
W!			/4 C822 /5 1234			
SF			R 0000			
Example 2: x0	)R W2, #0:	×1F, [W8++]	'	by 0x1F (W	,	
				esult to [N crement W8	W8]	
	Defens					
	Before		After Instruction			
	Instruction		IIISUUCUUII			
W		W	/2 8505			
W: W: Data 100/	2 8505 8 1004		/2 8505 /8 1006			

XOR	Exclusive OR Wb and Ws							
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F	dsPIC33F	dsPIC33E		
	Х	Х	Х	Х	Х	Х		
Syntax:	{label:}	XOR{.B}	Wb,	Ws,	Wd			
				[Ws],	[Wd]			
				[Ws++],	[Wd++]			
				[Ws],	[Wd]			
				[++Ws],	[++Wd]			
				[Ws],	[Wd]			
Operands:	Wb ∈ [W0 Ws ∈ [W0 Wd ∈ [W0	W15]						
Operation:	(Wb).XOR	(Wb).XOR.(Ws) $\rightarrow$ Wd						
Status Affected:	N, Z							
Encoding:	0110	1www	wBqq	qddd	dppp	SSSS		
Description:	Compute the logical exclusive OR operation of the contents of the source register Ws and the contents of the base register Wb, and place the result in the destination register Wd. Register direct addressing must be used for Wb. Either register direct or indirect addressing may be used for Ws and Wd.							
	The 'B' bit The 'q' bits The 'd' bits The 'p' bits	s select the a selects byte o select the de select the de select the so select the so	or word oper estination Ad estination reg ource Addres	ation ('0' for dress mode. gister. ss mode.	word, '1' for I	oyte).		
	Note:		a word opera	tion. You ma	lenotes a byta ay use a .W e required.			
Words:	1							
Cycles:	1 <sup>(1)</sup>							

In dsPIC33E and PIC24E devices, the listed cycle count does not apply to read an read-modify-write operations on non-CPU Special Function Registers. For more details, see Note 3 in Section 3.2.1 "Multi-Cycle Instructions".

Example 1:	XOR.B	W1,	[W5++],	[W9++]	; Stor	W1 and [W5] (Byte mode) e result to [W9] -increment W5 and W9
Data Data	Ins W1 / W5 / W9 / 2000 /	efore tructio AAAA 2000 2600 115A 0000 0000		W1 W5 W9 Pata 2000 Pata 2600 SR	After Instructi 2001 2601 1154 00F0 0008	
<u>Example 2:</u>	Be Instr W1 I W5	21, W5 efore uction EDC 1234 A34D 0000		; S1		2 4 3

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# **16-bit MCU and DSC Programmer's Reference Manual**

lana la an a sata al ins.	DIGO4E	DIODALL	DIGD4E			
Implemented in:	PIC24F	PIC24H	PIC24E	dsPIC30F X	dsPIC33F	dsPIC33E
	Х	Х	Х	X	Х	Х
Syntax:	{label:}	ZE	Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws],	Wnd		
Operands:	$Ws \in [W0]$ Wnd $\in [W0]$					
Operation:	Ws<7:0> →Wnd<7:0> 0 →Wnd<15:8>					
Status Affected:						
Encoding:	1111 1011			0ddd	dppp	SSSS
Description:	a 16-bit va Wnd. Eithe and registe	lue and store er register dir er direct addr	e the result in ect or indirect essing must	yte in source the destinati addressing be used for N se the zero-e	on working r may be used Vnd. The N f	egister d for Ws, lag is
	The 'p' bits	select the descent select the sel	ource Addres	ss mode.		
	Note 1:	_				
		The source \ address mod		sed as a byte y '1'.	e operand, so	o any
Words:	1					
Cycles:	1 <sup>(1)</sup>					
read-mod	33E and PIC2 lify-write oper ee <b>Note 3</b> in <b>5</b>	ations on nor	n-CPU Speci	al Function R	egisters. For	
Example 1: ZE		zero-extend				

<u>1.</u> 2	L V	10,	vv-	'		result	to W4		
		Be	fore				After		
	Instruction				Instruction				
	W3	7	'839			W3	7839		
	W4	1	.005			W4	0039		
	SR	0	0000			SR	0001	(C = 1)	

W2++], W12	; Store to	W12	2
Before Instruction	I	After nstructior	า
0900	W2	0901	
1002	W12	008F	
268F	Data 0900	268F	
0000	SR	0001	(C = 1)
	Before Instruction 0900 1002 268F	; Store to ; Post-incr Before Instruction I 0900 W2 1002 W12 268F Data 0900	Instruction         Instruction           0900         W2         0901           1002         W12         008F           268F         Data 0900         268F

NOTES:



# **Section 6. Built-in Functions**

# HIGHLIGHTS

This section of the manual contains the following major topics:

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6.2	Built-in Function List	447

#### 6.1 INTRODUCTION

This section describes the built-in functions that are specific to the MPLAB C Compiler for PIC24 MCUs and dsPIC DSCs (formerly MPLAB C30).

Built-in functions give the C programmer access to assembler operators or machine instructions that are currently only accessible using in-line assembly, but are sufficiently useful that they are applicable to a broad range of applications. Built-in functions are coded in C source files syntactically like function calls, but they are compiled to assembly code that directly implements the function, and do not involve function calls or library routines.

There are a number of reasons why providing built-in functions is preferable to requiring programmers to use in-line assembly. They include the following:

- 1. Providing built-in functions for specific purposes simplifies coding.
- 2. Certain optimizations are disabled when in-line assembly is used. This is not the case for built-in functions.
- З. For machine instructions that use dedicated registers, coding in-line assembly while avoiding register allocation errors can require considerable care. The built-in functions make this process simpler as you do not need to be concerned with the particular register requirements for each individual machine instruction.

The built-in functions are listed below followed by their individual detailed descriptions.

- builtin addab
- builtin add
- \_builtin\_btg
- builtin clr
- builtin clr prefetch
- \_builtin\_divf
- builtin divmodsd
- builtin divmodud
- \_builtin\_divsd
- builtin divud
- builtin dmaoffset
- \_\_builtin\_ed
- builtin edac
- builtin edsoffset
- builtin edspage
- builtin fbcl
- builtin lac
- builtin mac
- builtin modsd
- builtin modud
- builtin movsac
- builtin mpy

- builtin mpyn
- builtin msc
- builtin mulss
- builtin mulsu
- builtin mulus
- \_builtin\_muluu
- builtin nop
- builtin psvpage
- \_builtin\_psvoffset
- builtin readsfr
- builtin return address
- \_\_builtin\_sac
- builtin sacr
- builtin sftac
- builtin subab
- builtin tbladdress
- builtin tblpage
- builtin tbloffset
- builtin tblrdh
- builtin tblwth
- builtin tblwtl

This section describes only the built-in functions related to the CPU operations. The compiler provides additional built-in functions for operations such as writing to Flash program memory and changing the oscillator settings. Refer to the "MPLAB<sup>®</sup> C Compiler for PIC24 MCUs and dsPIC<sup>®</sup> DSCs User's Guide" (DS51284) for a complete list of compiler built-in functions.

- builtin tblrdl

# 6.2 BUILT-IN FUNCTION LIST

This section describes the programmer interface to the compiler built-in functions. Since the functions are "built-in", there are no header files associated with them. Similarly, there are no command-line switches associated with the built-in functions – they are always available. The built-in function names are chosen such that they belong to the compiler's namespace (they all have the prefix \_\_builtin\_), so they will not conflict with function or variable names in the programmer's namespace.

# \_builtin\_addab

#### **Description:**

Add accumulators A and B with the result written back to the specified accumulator. For example:

```
register int result asm("A");
register int B asm("A");
```

result = \_\_builtin\_addab(result,B);

will generate:

add A

Prototype:

int \_\_builtin\_addab(int Accum\_a, int Accum\_b);

#### Argument:

Accum\_a First accumulator to add. Accum\_b Second accumulator to add.

**Return Value:** 

Returns the addition result to an accumulator.

#### Assembler Operator / Machine Instruction:

add

Error Messages:

An error message appears if the result is not an accumulator register.

# \_builtin\_add

#### **Description:**

Add value to the accumulator specified by result with a shift specified by literal shift. For example:

register int result asm("A"); int value; result = \_\_builtin\_add(result,value,0);

If value is held in w0, the following will be generated:

add w0, #0, A

#### Prototype:

int \_\_builtin\_add(int Accum,int value, const int shift);

#### Argument:

Accum Accumulator to add.

- value Integer number to add to accumulator value.
- *shift* Amount to shift resultant accumulator value.

#### Return Value:

Returns the shifted addition result to an accumulator.

#### Assembler Operator / Machine Instruction:

add

#### Error Messages:

- · the result is not an accumulator register
- argument 0 is not an accumulator
- the shift value is not a literal within range

# **6** Built-in Functions

# \_\_builtin\_btg

#### **Description:**

```
This function will generate a btg machine instruction. Some examples include:
       /* near by default */
int i;
int l __attribute__((far));
struct foo {
  int bit1:1;
} barbits;
int bar;
void some_bittoggles() {
  register int j asm("w9");
  int k;
  k = i;
   _builtin_btg(&i,1);
  __builtin_btg(&j,3);
  __builtin_btg(&k,4);
  __builtin_btg(&l,11);
  return j+k;
```

}

Note that taking the address of a variable in a register will produce warning by the compiler and cause the register to be saved onto the stack (so that its address may be taken); this form is not recommended. This caution only applies to variables explicitly placed in registers by the programmer.

## Prototype:

```
void __builtin_btg(unsigned int *, unsigned int 0xn);
```

#### Argument:

\* A pointer to the data item for which a bit should be toggled.

0xn A literal value in the range of 0 to 15.

# **Return Value:**

Returns a btg machine instruction.

Assembler Operator / Machine Instruction:

btg

#### Error Messages:

An error message appears if the parameter values are not within range.

# \_builtin\_clr

## **Description:**

Clear the specified accumulator. For example:

```
register int result asm("A");
result = __builtin_clr();
```

will generate:

clr A

Prototype:

int \_\_builtin\_clr(void);

Argument:

None

**Return Value:** 

Returns the cleared value result to an accumulator.

Assembler Operator / Machine Instruction:

clr

Error Messages:

An error message appears if the result is not an accumulator register.

# \_\_builtin\_clr\_prefetch

#### **Description:**

Clear an accumulator and prefetch data ready for a future MAC operation.

*xptr* may be null to signify no X prefetch to be performed, in which case the values of *xincr* and *xval* are ignored, but required.

*yptr* may be null to signify no Y prefetch to be performed, in which case the values of *yincr* and *yval* are ignored, but required.

xval and yval nominate the address of a C variable where the prefetched value will be stored.

xincr and yincr may be the literal values: -6, -4, -2, 0, 2, 4, 6 or an integer value.

If AWB is non null, the other accumulator will be written back into the referenced variable.

For example:

```
register int result asm("A");
register int B asm("B");
int x_memory_buffer[256]
__attribute__((space(xmemory)));
int y_memory_buffer[256]
__attribute__((space(ymemory)));
int *xmemory;
int *ymemory;
int awb;
int xVal, yVal;
xmemory = x_memory_buffer;
ymemory = y_memory_buffer;
result = __builtin_clr(&xmemory, &xVal, 2,
```

&ymemory, &yVal, 2, &awb, B);

May generate:

clr A, [w8]+=2, w4, [w10]+=2, w5, w13

The compiler may need to spill w13 to ensure that it is available for the write-back. It may be recommended to users that the register be claimed for this purpose.

After this instruction:

- · result will be cleared
- xVal will contain x\_memory\_buffer[0]
- yVal will contain y\_memory\_buffer[0]
- xmemory and ymemory will be incremented by 2, ready for the next mac operation

#### Prototype:

```
int __builtin_clr_prefetch(
int **xptr, int *xval, int xincr,
int **yptr, int *yval, int yincr, int *AWB,
int AWB_accum);
```

# \_builtin\_clr\_prefetch (Continued)

#### Argument:

xptr	Integer pointer to x prefetch.
xval	Integer value of x prefetch.
xincr	Integer increment value of x prefetch.
yptr	Integer pointer to y prefetch.
yval	Integer value of y prefetch.
yincr	Integer increment value of y prefetch.
AWB	Accumulator write back location.
AWB_accum	Accumulator to write back.

**Note:** The arguments *xptr* and *yptr* must point to the arrays located in the x data memory and y data memory, respectively.

#### **Return Value:**

Returns the cleared value result to an accumulator.

Assembler Operator / Machine Instruction:

clr

#### **Error Messages:**

- · the result is not an accumulator register
- xval is a null value but xptr is not null
- yval is a null value but yptr is not null
- AWB\_accum is not an accumulator and AWB is not null

# \_builtin\_divf

#### **Description:**

Computes the quotient *num / den*. A math error exception occurs if *den* is zero. Function arguments are unsigned, as is the function result.

#### Prototype:

unsigned int \_\_builtin\_divf(unsigned int num, unsigned int den);

#### Argument:

*num* numerator *den* denominator

#### **Return Value:**

Returns the unsigned integer value of the quotient num / den.

Assembler Operator / Machine Instruction:

div.f

# \_builtin\_divmodsd

#### **Description:**

Issues the 16-bit architecture's native signed divide support. Notably, if the quotient does not fit into a 16-bit result, the results (including remainder) are unexpected. This form of the built-in function will capture both the quotient and remainder.

#### Prototype:

signed int \_\_builtin\_divmodsd(
signed long dividend, signed int divisor,
signed int \*remainder);

#### Argument:

*dividend* number to be divided *divisor* number to divide by *remainder* pointer to remainder

#### **Return Value:**

Quotient and remainder.

#### Assembler Operator / Machine Instruction:

divmodsd

Error Messages:

None.

## \_builtin\_divmodud

#### **Description:**

Issues the 16-bit architecture's native unsigned divide support. Notably, if the quotient does not fit into a 16-bit result, the results (including remainder) are unexpected. This form of the built-in function will capture both the quotient and remainder.

#### Prototype:

unsigned int \_\_builtin\_divmodud( unsigned long dividend, unsigned int divisor, unsigned int \*remainder);

#### Argument:

dividend	number to be divided
divisor	number to divide by
remainder	pointer to remainder

#### **Return Value:**

Quotient and remainder.

Assembler Operator / Machine Instruction:

divmodud

Error Messages:

None.

# \_builtin\_divsd

#### Description:

Computes the quotient *num / den*. A math error exception occurs if *den* is zero. Function arguments are signed, as is the function result. The command-line option -Wconversions can be used to detect unexpected sign conversions.

#### Prototype:

int \_\_builtin\_divsd(const long num, const int den);

#### Argument:

*num* numerator *den* denominator

#### **Return Value:**

Returns the signed integer value of the quotient num / den.

Assembler Operator / Machine Instruction:

div.sd

# \_builtin\_divud

#### **Description:**

Computes the quotient *num / den*. A math error exception occurs if *den* is zero. Function arguments are unsigned, as is the function result. The command-line option -Wconversions can be used to detect unexpected sign conversions.

#### Prototype:

unsigned int \_\_builtin\_divud(const unsigned long num, const unsigned int den);

#### Argument:

*num* numerator *den* denominator

#### Return Value:

Returns the unsigned integer value of the quotient num / den.

Assembler Operator / Machine Instruction:

div.ud

## \_builtin\_dmaoffset

#### **Description:**

Obtains the offset of a symbol within DMA memory. For example: unsigned int result; char buffer[256] \_\_attribute\_\_((space(dma))); result = \_\_builtin\_dmaoffset(&buffer); May generate: mov #dmaoffset(buffer), w0 Prototype: unsigned int \_\_builtin\_dmaoffset(const void \*p); Argument: \*p pointer to DMA address value **Return Value:** Returns the offset to a variable located in DMA memory. **Assembler Operator / Machine Instruction:** dmaoffset Error Messages: An error message appears if the parameter is not the address of a global symbol.

# \_builtin\_ed

#### **Description:**

Squares sqr, returning it as the result. Also prefetches data for future square operation by computing \*\*xptr - \*\*yptr and storing the result in \*distance.

xincr and yincr may be the literal values: -6, -4, -2, 0, 2, 4, 6 or an integer value.

For example:

```
register int result asm("A");
int *xmemory, *ymemory;
int distance;
```

&distance);

May generate:

ed w4\*w4, A, [w8]+=2, [W10]+=2, w4

#### Prototype:

int \_\_builtin\_ed(int sqr, int \*\*xptr, int xincr, int \*\*yptr, int yincr, int \*distance);

#### Argument:

sqr	Integer squared value.
xptr	Integer pointer to pointer to x prefetch.
xincr	Integer increment value of x prefetch.
yptr	Integer pointer to pointer to y prefetch.
yincr	Integer increment value of y prefetch.
distance	Integer pointer to distance.

**Note:** The arguments *xptr* and *yptr* must point to the arrays located in the x data memory and y data memory, respectively.

#### **Return Value:**

Returns the squared result to an accumulator.

#### Assembler Operator / Machine Instruction:

ed

#### Error Messages:

- · the result is not an accumulator register
- xptr is null
- yptr is null
- distance is null

# \_\_builtin\_edac

#### **Description:**

Squares sqr and sums with the nominated accumulator register, returning it as the result. Also prefetches data for future square operation by computing \*\*xptr - \*\*yptr and storing the result in \*distance.

xincr and yincr may be the literal values: -6, -4, -2, 0, 2, 4, 6 or an integer value.

For example:

register int result asm("A"); int \*xmemory, \*ymemory; int distance;

&ymemory, 2, &distance);

May generate:

edac w4\*w4, A, [w8]+=2, [W10]+=2, w4

#### Prototype:

int \_\_builtin\_edac(int Accum, int sqr, int \*\*xptr, int xincr, int \*\*yptr, int yincr, int \*distance);

#### Argument:

Accum	Accumulator to sum.
sqr	Integer squared value.
xptr	Integer pointer to pointer to x prefetch.
xincr	Integer increment value of x prefetch.
yptr	Integer pointer to pointer to y prefetch.
yincr	Integer increment value of y prefetch.
distance	Integer pointer to distance.

**Note:** The arguments *xptr* and *yptr* must point to the arrays located in the x data memory and y data memory, respectively.

#### **Return Value:**

Returns the squared result to specified accumulator.

Assembler Operator / Machine Instruction:

edac

#### Error Messages:

- · the result is not an accumulator register
- Accum is not an accumulator register
- xptr is null
- yptr is null
- distance is null

# \_builtin\_edsoffset

#### **Description:**

Returns the eds page offset of the object whose address is given as a parameter. The argument p must be the address of an object in extended data space; otherwise an error message is produced and the compilation fails. See the space attribute in **Section 2.3.1 "Specifying Attributes of Variables"** of the "MPLAB<sup>®</sup> C Compiler for PIC24 MCUs and dsPIC<sup>®</sup> DSCs User's Guide" (DS51284).

#### Prototype:

unsigned int \_\_builtin\_edsoffset(int \*p);

#### Argument:

p object address

#### Return Value:

Returns the eds page number of the object whose address is given as a parameter

Assembler Operator / Machine Instruction:

edsoffset

# \_builtin\_edspage

#### Description:

Returns the eds page number of the object whose address is given as a parameter. The argument *p* must be the address of an object in extended data space; otherwise an error message is produced and the compilation fails. See the space attribute in **Section 2.3.1 "Specifying Attributes of Variables"** of the "MPLAB<sup>®</sup> C Compiler for PIC24 MCUs and dsPIC<sup>®</sup> DSCs User's Guide" (DS51284).

#### Prototype:

unsigned int \_\_builtin\_edspage(int \*p);

#### Argument:

*p* object address

#### **Return Value:**

Returns the eds page number of the object whose address is given as a parameter.

Assembler Operator / Machine Instruction:

edspage

# Section 6. Built-in Functions

# \_builtin\_fbcl

#### **Description:**

Finds the first bit change from left in value. This is useful for dynamic scaling of fixed-point data. For example:

int result, value; result = \_\_builtin\_fbcl(value);

May generate:

# fbcl w4, w5

Prototype:

int \_\_builtin\_fbcl(int value);

#### Argument:

*value* Integer number of first bit change.

#### **Return Value:**

Returns the shifted addition result to an accumulator.

Assembler Operator / Machine Instruction:

fbcl

#### Error Messages:

An error message appears if the result is not an accumulator register.

# \_builtin\_lac

#### **Description:**

Shifts value by *shift* (a literal between -8 and 7) and returns the value to be stored into the accumulator register. For example:

register int result asm("A"); int value; result = \_\_builtin\_lac(value,3);

May generate:

lac w4, #3, A

#### Prototype:

int \_\_builtin\_lac(int value, int shift);

#### Argument:

*value* Integer number to be shifted. *shift* Literal amount to shift.

# Return Value:

Returns the shifted addition result to an accumulator.

#### Assembler Operator / Machine Instruction:

lac

#### Error Messages:

- the result is not an accumulator register
- · the shift value is not a literal within range

# \_builtin\_mac

#### **Description:**

Computes  $a \times b$  and sums with accumulator; also prefetches data ready for a future MAC operation.

*xptr* may be null to signify no X prefetch to be performed, in which case the values of *xincr* and *xval* are ignored, but required.

*yptr* may be null to signify no Y prefetch to be performed, in which case the values of *yincr* and *yval* are ignored, but required.

xval and yval nominate the address of a C variable where the prefetched value will be stored.

xincr and yincr may be the literal values: -6, -4, -2, 0, 2, 4, 6 or an integer value.

If AWB is non null, the other accumulator will be written back into the referenced variable.

For example:

```
register int result asm("A");
register int B asm("B");
int *xmemory;
int *ymemory;
int xVal, yVal;
result = __builtin_mac(result, xVal, yVal,
&xmemory, &xVal, 2,
&ymemory, &yVal, 2, 0, B);
May generate:
```

mac w4\*w5, A, [w8]+=2, w4, [w10]+=2, w5

Prototype:

int \_\_builtin\_mac(int Accum, int a, int b, int \*\*xptr, int \*xval, int xincr, int \*\*yptr, int \*yval, int yincr, int \*AWB, int AWB\_accum);

#### Argument:

Accum	Accumulator to sum.
а	Integer multiplicand.
b	Integer multiplier.
xptr	Integer pointer to pointer to x prefetch.
xval	Integer pointer to value of x prefetch.
xincr	Integer increment value of x prefetch.
yptr	Integer pointer to pointer to y prefetch.
yval	Integer pointer to value of y prefetch.
yincr	Integer increment value of y prefetch.
AWB	Accumulator write-back location.
AWB_accum	Accumulator to write-back.

**Note:** The arguments *xptr* and *yptr* must point to the arrays located in the x data memory and y data memory, respectively.

#### **Return Value:**

Returns the cleared value result to an accumulator.

Assembler Operator / Machine Instruction:

mac

# \_\_builtin\_mac (Continued)

#### Error Messages:

- the result is not an accumulator register
- Accum is not an accumulator register
- *xval* is a null value but *xptr* is not null
- *yval* is a null value but *yptr* is not null
- AWB\_accum is not an accumulator register and AWB is not null

# \_builtin\_modsd

#### **Description:**

Issues the 16-bit architecture's native signed divide support. Notably, if the quotient does not fit into a 16-bit result, the results (including remainder) are unexpected. This form of the built-in function will capture only the remainder.

#### Prototype:

signed int \_\_builtin\_modsd(signed long dividend, signed int divisor);

#### Argument:

*dividend* number to be divided *divisor* number to divide by

**Return Value:** 

Remainder.

Assembler Operator / Machine Instruction:

modsd

**Error Messages:** 

None.

# \_builtin\_modud

#### **Description:**

Issues the 16-bit architecture's native unsigned divide support. Notably, if the quotient does not fit into a 16-bit result, the results (including remainder) are unexpected. This form of the built-in function will capture only the remainder.

#### Prototype:

unsigned int \_\_builtin\_modud(unsigned long dividend, unsigned int divisor);

#### Argument:

*dividend* number to be divided *divisor* number to divide by

#### **Return Value:**

Remainder.

Assembler Operator / Machine Instruction:

modud

Error Messages:

None.

# Section 6. Built-in Functions

# \_\_builtin\_movsac

#### **Description:**

Computes nothing, but prefetches data ready for a future MAC operation.

*xptr* may be null to signify no X prefetch to be performed, in which case the values of *xincr* and *xval* are ignored, but required.

*yptr* may be null to signify no Y prefetch to be performed, in which case the values of *yincr* and *yval* are ignored, but required.

xval and yval nominate the address of a C variable where the prefetched value will be stored.

xincr and yincr may be the literal values: -6, -4, -2, 0, 2, 4, 6 or an integer value.

If AWB is not null, the other accumulator will be written back into the referenced variable.

For example:

```
register int result asm("A");
int *xmemory;
int *ymemory;
int xVal, yVal;
result = __builtin_movsac(&xmemory, &xVal, 2,
```

```
&ymemory, &yVal, 2, 0, 0);
```

May generate:

```
movsac A, [w8]+=2, w4, [w10]+=2, w5
```

#### Prototype:

int \_\_builtin\_movsac(
int \*\*xptr, int \*xval, int xincr,
int \*\*yptr, int \*yval, int yincr, int \*AWB
int AWB\_accum);

#### Argument:

xptr	Integer pointer to pointer to x prefetch.
xval	Integer pointer to value of x prefetch.
xincr	Integer increment value of x prefetch.
yptr	Integer pointer to pointer to y prefetch.
yval	Integer pointer to value of y prefetch.
yincr	Integer increment value of y prefetch.
AWB	Accumulator write back location.
AWB_accum	Accumulator to write back.

**Note:** The arguments *xptr* and *yptr* must point to the arrays located in the x data memory and y data memory, respectively.

#### **Return Value:**

Returns prefetch data.

Assembler Operator / Machine Instruction:

movsac

#### Error Messages:

- · the result is not an accumulator register
- xval is a null value but xptr is not null
- yval is a null value but yptr is not null
- AWB\_accum is not an accumulator register and AWB is not null

# \_builtin\_mpy

#### **Description:**

Computes  $a \times b$ ; also prefetches data ready for a future MAC operation.

*xptr* may be null to signify no X prefetch to be performed, in which case the values of *xincr* and *xval* are ignored, but required.

*yptr* may be null to signify no Y prefetch to be performed, in which case the values of *yincr* and *yval* are ignored, but required.

xval and yval nominate the address of a C variable where the prefetched value will be stored.

xincr and yincr may be the literal values: -6, -4, -2, 0, 2, 4, 6 or an integer value.

For example:

```
register int result asm("A");
int *xmemory;
int *ymemory;
int xVal, yVal;
result = __builtin_mpy(xVal, yVal,
&xmemory, &xVal, 2,
&ymemory, &yVal, 2);
```

May generate:

```
mac w4*w5, A, [w8]+=2, w4, [w10]+=2, w5
```

Prototype:

```
int __builtin_mpy(int a, int b,
int **xptr, int *xval, int xincr,
int **yptr, int *yval, int yincr);
```

#### Argument:

а	Integer multiplicand.
b	Integer multiplier.
xptr	Integer pointer to pointer to x prefetch.
xval	Integer pointer to value of x prefetch.
xincr	Integer increment value of x prefetch.
yptr	Integer pointer to pointer to y prefetch.
yval	Integer pointer to value of y prefetch.
yincr	Integer increment value of y prefetch.
AWB	Integer pointer to accumulator selection.

**Note:** The arguments *xptr* and *yptr* must point to the arrays located in the x data memory and y data memory, respectively.

#### **Return Value:**

Returns the cleared value result to an accumulator.

Assembler Operator / Machine Instruction:

mpy

#### Error Messages:

- the result is not an accumulator register
- xval is a null value but xptr is not null
- yval is a null value but yptr is not null

# Section 6. Built-in Functions

# \_builtin\_mpyn

#### **Description:**

Computes  $-a \times b$ ; also prefetches data ready for a future MAC operation.

*xptr* may be null to signify no X prefetch to be performed, in which case the values of *xincr* and *xval* are ignored, but required.

*yptr* may be null to signify no Y prefetch to be performed, in which case the values of *yincr* and *yval* are ignored, but required.

xval and yval nominate the address of a C variable where the prefetched value will be stored.

xincr and yincr may be the literal values: -6, -4, -2, 0, 2, 4, 6 or an integer value.

For example:

register int result asm("A"); int \*xmemory; int \*ymemory; int xVal, yVal;

May generate:

mac w4\*w5, A, [w8]+=2, w4, [w10]+=2, w5

Prototype:

int \_\_builtin\_mpyn(int a, int b, int \*\*xptr, int \*xval, int xincr, int \*\*yptr, int \*yval, int yincr);

#### Argument:

а	Integer multiplicand.
b	Integer multiplier.
xptr	Integer pointer to pointer to x prefetch.
xval	Integer pointer to value of x prefetch.
xincr	Integer increment value of x prefetch.
yptr	Integer pointer to pointer to y prefetch.
yval	Integer pointer to value of y prefetch.
yincr	Integer increment value of y prefetch.
AWB	Integer pointer to accumulator selection.

**Note:** The arguments *xptr* and *yptr* must point to the arrays located in the x data memory and y data memory, respectively.

#### **Return Value:**

Returns the cleared value result to an accumulator.

Assembler Operator / Machine Instruction:

mpyn

#### Error Messages:

- · the result is not an accumulator register
- *xval* is a null value but *xptr* is not null
- yval is a null value but yptr is not null

# \_builtin\_msc

#### **Description:**

Computes  $a \times b$  and subtracts from accumulator; also prefetches data ready for a future MAC operation.

*xptr* may be null to signify no X prefetch to be performed, in which case the values of *xincr* and *xval* are ignored, but required.

*yptr* may be null to signify no Y prefetch to be performed, in which case the values of *yincr* and *yval* are ignored, but required.

xval and yval nominate the address of a C variable where the prefetched value will be stored.

xincr and yincr may be the literal values: -6, -4, -2, 0, 2, 4, 6 or an integer value.

If AWB is non null, the other accumulator will be written back into the referenced variable.

For example:

```
register int result asm("A");
int *xmemory;
int *ymemory;
int xVal, yVal;
result = __builtin_msc(result, xVal, yVal,
                       &xmemory, &xVal, 2,
                       &ymemory, &yVal, 2, 0, 0);
May generate:
msc w4*w5, A, [w8]+=2, w4, [w10]+=2, w5
Prototype:
    __builtin_msc(int Accum, int a, int b,
int
int **xptr, int *xval, int xincr,
int **yptr, int *yval, int yincr, int *AWB,
int AWB_accum);
Argument:
            IAccumulator to sum.
Accum
            Integer multiplicand.
а
```

b	Integer multiplier.
xptr	Integer pointer to pointer to x prefetch.
xval	Integer pointer to value of x prefetch.
xincr	Integer increment value of x prefetch.
yptr	Integer pointer to pointer to y prefetch.
yval	Integer pointer to value of y prefetch.
yincr	Integer increment value of y prefetch.
AWB	Accumulator write back location.
AWB_accum	Accumulator to write back.

**Note:** The arguments *xptr* and *yptr* must point to the arrays located in the x data memory and y data memory, respectively.

#### **Return Value:**

Returns the cleared value result to an accumulator.

Assembler Operator / Machine Instruction:

msc

# \_builtin\_msc (Continued)

#### Error Messages:

- the result is not an accumulator register
- Accum is not an accumulator register
- *xval* is a null value but *xptr* is not null
- *yval* is a null value but *yptr* is not null
- AWB\_accum is not an accumulator register and AWB is not null

## \_builtin\_mulss

#### **Description:**

Computes the product  $p\theta \times p1$ . Function arguments are signed integers, and the function result is a signed long integer. The command-line option -Wconversions can be used to detect unexpected sign conversions.

#### Prototype:

signed long \_\_builtin\_mulss(const signed int p0, const signed int p1);

#### Argument:

- *p0* multiplicand
- *p1* multiplier

### Return Value:

Returns the signed long integer value of the product  $p0 \times p1$ .

Assembler Operator / Machine Instruction:

mul.ss

# \_builtin\_mulsu

#### **Description:**

Computes the product  $p0 \times p1$ . Function arguments are integers with mixed signs, and the function result is a signed long integer. The command-line option -Wconversions can be used to detect unexpected sign conversions. This function supports the full range of addressing modes of the instruction, including immediate mode for operand p1.

#### Prototype:

signed long \_\_builtin\_mulsu(const signed int p0, const unsigned int p1);

# Argument:

*p0* multiplicand*p1* multiplier

# **Return Value:**

Returns the signed long integer value of the product  $p0 \times p1$ .

Assembler Operator / Machine Instruction:

mul.su
## \_builtin\_mulus

#### **Description:**

Computes the product  $p0 \times p1$ . Function arguments are integers with mixed signs, and the function result is a signed long integer. The command-line option -Wconversions can be used to detect unexpected sign conversions. This function supports the full range of addressing modes of the instruction.

#### Prototype:

signed long \_\_builtin\_mulus(const unsigned int p0, const signed int p1);

#### Argument:

*p0* multiplicand

*p1* multiplier

#### Return Value:

Returns the signed long integer value of the product  $p0 \times p1$ .

#### Assembler Operator / Machine Instruction:

mul.us

## \_builtin\_muluu

#### **Description:**

Computes the product  $p0 \times p1$ . Function arguments are unsigned integers, and the function result is an unsigned long integer. The command-line option -Wconversions can be used to detect unexpected sign conversions. This function supports the full range of addressing modes of the instruction, including immediate mode for operand p1.

#### Prototype:

unsigned long \_\_builtin\_muluu(const unsigned int p0, const unsigned int p1);
Argument:

## Argument:

- *p0* multiplicand
- *p1* multiplier

### **Return Value:**

Returns the signed long integer value of the product  $p0 \times p1$ .

Assembler Operator / Machine Instruction:

mul.uu

## \_builtin\_nop

Description: Generates a nop instruction. Prototype: void \_\_builtin\_nop(void); Argument: None. Return Value: Returns a no operation (nop). Assembler Operator / Machine Instruction: nop

## \_builtin\_psvoffset

#### Description:

Returns the psv page offset of the object whose address is given as a parameter. The argument p must be the address of an object in an EE data, PSV or executable memory space; otherwise an error message is produced and the compilation fails. See the space attribute in **Section 2.3.1 "Specifying Attributes of Variables"** of the "MPLAB<sup>®</sup> C Compiler for PIC24 MCUs and dsPIC<sup>®</sup> DSCs User's Guide" (DS51284).

Prototype:

```
unsigned int __builtin_psvoffset(const void *p);
```

Argument:

*p* object address

**Return Value:** 

Returns the psv page number offset of the object whose address is given as a parameter.

Assembler Operator / Machine Instruction:

psvoffset

#### Error Messages:

The following error message is produced when this function is used incorrectly:

"Argument to \_\_builtin\_psvoffset() is not the address of an object in code, psv, or eedata section".

The argument must be an explicit object address.

For example, if *obj* is object in an executable or read-only section, the following syntax is valid: unsigned page = \_\_builtin\_psvoffset(&obj);

## \_builtin\_psvpage

#### **Description:**

Returns the psv page number of the object whose address is given as a parameter. The argument *p* must be the address of an object in an EE data, PSV or executable memory space; otherwise an error message is produced and the compilation fails. See the space attribute in **Section 2.3.1 "Specifying Attributes of Variables"** of the "*MPLAB*<sup>®</sup> *C Compiler for PIC24 MCUs and dsPIC*<sup>®</sup> *DSCs User's Guide*" (DS51284).

#### Prototype:

unsigned int \_\_builtin\_psvpage(const void \*p);

#### Argument:

p object address

#### **Return Value:**

Returns the psv page number of the object whose address is given as a parameter.

#### Assembler Operator / Machine Instruction:

psvpage

#### Error Messages:

The following error message is produced when this function is used incorrectly:

"Argument to \_\_builtin\_psvpage() is not the address of an object in code, psv, or eedata section".

The argument must be an explicit object address.

For example, if *obj* is object in an executable or read-only section, the following syntax is valid:

unsigned page = \_\_builtin\_psvpage(&obj);

## \_builtin\_readsfr

## Description:

Reads the SFR.
Prototype:
unsigned int \_\_builtin\_readsfr(const void \*p);
Argument:
p object address
Return Value:
Returns the SFR.
Assembler Operator / Machine Instruction:
readsfr
Error Messages:
The following error measure is produced when this function is used in

The following error message is produced when this function is used incorrectly:

### \_builtin\_return\_address

#### **Description:**

Returns the return address of the current function, or of one of its callers. For the *level* argument, a value of 0 yields the return address of the current function, a value of 1 yields the return address of the caller of the current function, and so forth. When level exceeds the current stack depth, 0 will be returned. This function should only be used with a non-zero argument for debugging purposes.

#### Prototype:

int \_\_builtin\_return\_address (const int level);

#### Argument:

*level* Number of frames to scan up the call stack.

### **Return Value:**

Returns the return address of the current function, or of one of its callers.

#### Assembler Operator / Machine Instruction:

return\_address

## \_builtin\_sac

#### Description:

Shifts value by *shift* (a literal between -8 and 7) and returns the value.

For example:

```
register int value asm("A");
int result;
```

result = \_\_builtin\_sac(value,3);

May generate:

sac A, #3, w0

#### Prototype:

int \_\_builtin\_sac(int value, int shift);

#### Argument:

valueInteger number to be shifted.shiftLiteral amount to shift.

### Return Value:

Returns the shifted result to an accumulator.

Assembler Operator / Machine Instruction:

sac

#### Error Messages:

An error message appears if:

- the result is not an accumulator register
- the shift value is not a literal within range

## \_builtin\_sacr

#### **Description:**

Shifts value by *shift* (a literal between -8 and 7) and returns the value which is rounded using the rounding mode determined by the CORCONbits.RND control bit.

For example:

register int value asm("A"); int result;

result = \_\_builtin\_sac(value,3);

May generate:

sac.r A, #3, w0

Prototype:

int \_\_builtin\_sacr(int value, int shift);

Argument:

*value* Integer number to be shifted. *shift* Literal amount to shift.

**Return Value:** 

Returns the shifted result to the CORCON register.

Assembler Operator / Machine Instruction:

sacr

#### Error Messages:

An error message appears if:

- · the result is not an accumulator register
- the shift value is not a literal within range

## \_builtin\_sftac

#### **Description:**

Shifts accumulator by *shift*. The valid shift range is -16 to 16.

For example:

register int result asm("A");
int i;

result = \_\_builtin\_sftac(result,i);

May generate:

sftac A, w0

Prototype:

int \_\_builtin\_sftac(int Accum, int shift);

#### Argument:

Accum Accumulator to shift. shift Amount to shift.

#### **Return Value:**

Returns the shifted result to an accumulator.

Assembler Operator / Machine Instruction:

sftac

#### Error Messages:

An error message appears if:

- · the result is not an accumulator register
- Accum is not an accumulator register
- the shift value is not a literal within range

## \_builtin\_subab

#### **Description:**

Subtracts accumulators A and B with the result written back to the specified accumulator. For example:

```
register int result asm("A");
register int B asm("B");
result = __builtin_subab(result,B);
```

will generate:

sub A

#### Prototype:

int \_\_\_\_builtin\_subab(int Accum\_a, int Accum\_b);

#### Argument:

Accum\_aAccumulator from which to subtract.Accum\_bAccumulator to subtract.

**Return Value:** 

Returns the subtraction result to an accumulator.

Assembler Operator / Machine Instruction:

sub

#### Error Messages:

An error message appears if the result is not an accumulator register.

### \_builtin\_tbladdress

#### **Description:**

Returns a value that represents the address of an object in program memory. The argument p must be the address of an object in an EE data, PSV or executable memory space; otherwise an error message is produced and the compilation fails. See the space attribute in **Section 2.3.1 "Specifying Attributes of Variables"** of the "MPLAB<sup>®</sup> C Compiler for PIC24 MCUs and dsPIC<sup>®</sup> DSCs User's Guide" (DS51284).

#### Prototype:

unsigned long \_\_builtin\_tblpage(const void \*p);

#### Argument:

*p* object address

#### **Return Value:**

Returns an unsigned long value that represents the address of an object in program memory.

#### Assembler Operator / Machine Instruction:

tbladdress

## \_builtin\_tbladdress

#### Error Messages:

The following error message is produced when this function is used incorrectly:

"Argument to \_\_builtin\_tbladdress() is not the address of an object in code, psv, or eedata section".

The argument must be an explicit object address.

For example, if *obj* is object in an executable or read-only section, the following syntax is valid: unsigned long page = \_\_builtin\_tbladdress(&obj);

## \_builtin\_tbloffset

#### **Description:**

Returns the table page offset of the object whose address is given as a parameter. The argument *p* must be the address of an object in an EE data, PSV or executable memory space; otherwise an error message is produced and the compilation fails. See the space attribute in **Section 2.3.1 "Specifying Attributes of Variables"** of the "MPLAB<sup>®</sup> C Compiler for PIC24 MCUs and dsPIC<sup>®</sup> DSCs User's Guide" (DS51284).

#### Prototype:

unsigned int \_\_builtin\_tbloffset(const void \*p);

Argument:

p object address

**Return Value:** 

Returns the table page number offset of the object whose address is given as a parameter.

Assembler Operator / Machine Instruction:

tbloffset

#### Error Messages:

The following error message is produced when this function is used incorrectly:

"Argument to \_\_builtin\_tbloffset() is not the address of an object in code, psv, or eedata section".

The argument must be an explicit object address.

For example, if *obj* is object in an executable or read-only section, the following syntax is valid: unsigned page = \_\_builtin\_tbloffset(&obj);

## \_builtin\_tblpage

#### **Description:**

Returns the table page number of the object whose address is given as a parameter. The argument *p* must be the address of an object in an EE data, PSV or executable memory space; otherwise an error message is produced and the compilation fails. See the space attribute in **Section 2.3.1 "Specifying Attributes of Variables"** of the "*MPLAB*<sup>®</sup> *C Compiler for PIC24 MCUs and dsPIC*<sup>®</sup> *DSCs User's Guide*" (DS51284).

#### Prototype:

unsigned int \_\_builtin\_tblpage(const void \*p);

#### Argument:

p object address

#### Return Value:

Returns the table page number of the object whose address is given as a parameter.

#### Assembler Operator / Machine Instruction:

tblpage

#### Error Messages:

The following error message is produced when this function is used incorrectly:

"Argument to \_\_builtin\_tblpage() is not the address of an object in code, psv, or eedata section".

The argument must be an explicit object address.

For example, if obj is object in an executable or read-only section, the following syntax is valid:

unsigned page = \_\_builtin\_tblpage(&obj);

## \_builtin\_tblrdh

#### **Description:**

Issues the tblrdh.w instruction to read a word from Flash or EEDATA memory. You must set up the TBLPAG to point to the appropriate page. To do this, you may make use of \_\_builtin\_tbloffset() and \_\_builtin\_tblpage().

Please refer to the specific device data sheet or the appropriate family reference manual for complete details regarding reading and writing program Flash.

#### Prototype:

unsigned int \_\_builtin\_tblrdh(unsigned int offset);

#### Argument:

offset desired memory offset

**Return Value:** 

None.

Assembler Operator / Machine Instruction:

tblrdh

#### Error Messages:

None.

## \_builtin\_tblrdl

#### **Description:**

Issues the tblrdl.w instruction to read a word from Flash or EEDATA memory. You must set up the TBLPAG to point to the appropriate page. To do this, you may make use of \_\_builtin\_tbloffset() and\_\_builtin\_tblpage().

Please refer to the specific device data sheet or the appropriate family reference manual for complete details regarding reading and writing program Flash.

#### Prototype:

unsigned int \_\_builtin\_tblrdl(unsigned int offset);

Argument:

offset desired memory offset

**Return Value:** 

None.

Assembler Operator / Machine Instruction:

tblrdl

Error Messages:

None.

## \_builtin\_tblwth

#### **Description:**

Issues the tblwth.winstruction to write a word to Flash or EEDATA memory. You must set up the TBLPAG to point to the appropriate page. To do this, you may make use of \_\_builtin\_tbloffset() and \_\_builtin\_tblpage().

Please refer to the specific device data sheet or the appropriate family reference manual for complete details regarding reading and writing program Flash.

#### Prototype:

void \_\_builtin\_tblwth(unsigned int offset unsigned int data);

#### Argument:

offset desired memory offset data to be written

**Return Value:** 

None.

Assembler Operator / Machine Instruction:

tblwth

#### Error Messages:

None.

## \_builtin\_tblwtl

#### **Description:**

Issues the tblrdl.w instruction to write a word to Flash or EEDATA memory. You must set up the TBLPAG to point to the appropriate page. To do this, you may make use of \_\_builtin\_tbloffset() and \_\_builtin\_tblpage().

Please refer to the specific device data sheet or the appropriate family reference manual for complete details regarding reading and writing program Flash.

#### Prototype:

void \_\_builtin\_tblwtl(unsigned int offset unsigned int data);

#### Argument:

offset desired memory offset data data to be written

**Return Value:** 

None.

Assembler Operator / Machine Instruction:

tblwtl

Error Messages:

None.

```
Example 6-1:
                       Additional Inline Functions
 #include "p33fxxxx.h"
 volatile long Result_mpy1616;
 volatile long Result_addab;
 volatile long Result_subab
 volatile long Result_mpy3216;
 volatile long Result_div3216;
 register int Accu_A asm("A");
register int Accu_B asm("B");
 inline static long mpy_32_16 (long, int);
 inline static long mpy_32_16 (long x, int y)
 Ł
       long result;
      int temp1, temp2;
temp1 = (x>>1)&0x7FFF;
       temp2 = \dot{x} >> 16;
      Accu_A = __builtin_mpy (temp1, y, 0,0,0,0,0,0,0);
Accu_A = __builtin_sftac (15);
Accu_A = __builtin_mac (temp2, y, 0,0,0,0,0,0,0);
asm("mov _ACCAL,%0\n\t"
    "mov _ACCAH,%d0" : "=r"(result) : "w"(Accu_A));
       return result;
 }
 int main (void)
 {
       // Variable declarations
      int Input1;
int Input2;
      int Input3
int Input4
       long Input5;
       int Input6;
       long Input7;
       int Input8;
       // Enable 32-bit saturation, signed and fractional modes for both ACCA
             and ACCB
       CORCON = 0 \times 00C0;
       // Example of 16*16-bit fractional multiplication using ACCA
       Input1 = 32767;
       Input2 = 32767
      Accu_A = __builtin_mpy (Input1, Input2, 0,0,0,0,0,0);
asm("mov _ACCAL,%0\n\t"
"mov _ACCAH,%d0" : "=r"(Result_mpy1616) : "w"(Accu_A));
       // Example of 16*16-bit fractional multiplication using ACCB
       Input3 = 16384;
       Input4 = 16384
      Input = __builtin_mpy (Input3, Input4, 0,0,0,0,0,0);
asm("mov _ACCBL,%0\n\t"
"mov _ACCBH,%d0" : "=r"(Result_mpy1616) : "w"(Accu_B));
      // Example of 32-bit addition using ACCA (ACCA = ACCA + ACCB)
Accu_A = __builtin_addab();
asm("mov _ACCAL,%0\n\t"
"mov _ACCAH,%d0" : "=r"(Result_addab) : "w"(Accu_A));
      // Example of 32-bit subtraction using ACCB (ACCB = ACCB - ACCA)
Accu_B = __builtin_subab();
asm("mov _ACCBL,%0\n\t"
"mov _ACCBH,%d0" : "=r"(Result_subab) : "w"(Accu_B));
      // Example of 32*16-bit fractional multiplication using ACCA
Input5 = 0x7FFFFFF;
Input6 = 32767;
       Result_mpy3216 = mpy_32_16 (Input5, Input6);
       while(1);
 }
```

```
Example 6-2:
               Divide_32_by_16
#include <p33Fxxxx.h>
#include "divide.h"
_FOSCSEL(FNOSC_FRC);
_FOSC(FCKSM_CSDCMD & OSCIOFNC_OFF & POSCMD_NONE);
_FWDT(FWDTEN_OFF);
unsigned int divide_(long a, int b) {
  union convert {
    unsigned long 1;
    unsigned int i[2];
  } c;
  int sign;
  unsigned int result;
  c.l = a;
  sign = c.i[1] \wedge b;
  if (a < 0) a = (-a);
  if (b < 0) b = -b;
  result = __builtin_divud(a,b);
  result >>= 1;
  if (sign < 0) result = -result;</pre>
  return result;
}
int main(void)
{
    unsigned long dividend;
    unsigned int divisor;
    unsigned int quotient;
    dividend = 0x3FFFFFF;
    divisor = 0x7FFF;
    quotient = divide_((long)dividend, (int)divisor);
    while(1);
}
```

NOTES:



# **Section 7. Reference**

## HIGHLIGHTS

This section of the manual contains the following major topics:

7.1	Instruction Bit Map	. 484
7.2	Instruction Set Summary Table	. 486
7.3	Revision History	. 496

## 7.1 INSTRUCTION BIT MAP

Instruction encoding for the 16-bit MCU and DSC family devices is summarized in Table 7-1. This table contains the encoding for the MSB of each instruction. The first column in the table represents bits 23:20 of the opcode, and the first row of the table represents bits 19:16 of the opcode. The first byte of the opcode is formed by taking the first column bit value and appending the first row bit value. For instance, the MSB of the PUSH instruction (last row, ninth column) is encoded with 11111000b (0xF8).

**Note:** The complete opcode for each instruction may be determined by the instruction descriptions in **Section 5. "Instruction Descriptions"**, using Table 5-1 through Table 5-12.

Table 7-1:	nstruction Encoding
------------	---------------------

		inot			.9													
									Ор	code<19:16>								
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100				
	0000	NOP	BRA CALL GOTO RCALL	CALL	—	GOTO	RETLW	RETFIE RETURN	RCALL	DO <sup>(1)</sup>	REPEAT	—	—	BRA <sup>(1)</sup> (OA)				
	0001					SUBR							SUBBR					
	0010									MOV								
	0011	BRA (OV)	BRA (C)	BRA (Z)	BRA (N)	BRA (LE)	BRA (LT)	BRA (LEU)	BRA	BRA (NOV)	BRA (NC)	BRA (NZ)	BRA (NN)	BRA (GT)				
	0100					ADD							ADDC					
	0101					SUB			_				SUBB					
	0110					AND			_				XOR					
	0111					IOR							MOV					
	1000								_	MOV								
۵	1001									MOV								
3:2(	1010	BSET	BCLR	BTG	BTST	BTSTS	BTST	BTSS	BTSC	BSET	BCLR	BTG	BTST	BTSTS				
Opcode<23:20>	1011	ADD ADDC	SUB SUBB	AND XOR	IOR MOV	ADD ADDC	SUB SUBB	AND XOR	IOR MOV	MUL.US MUL.UU	MUL.SS MUL.SU	TBLRDH TBLRDL	TBLWTH TBLWTL	MUL				
Opc	1100		MAC <sup>(1)</sup> MPY <sup>(1)</sup> MPY.N <sup>(1)</sup> MSC <sup>(1)</sup>		CLRAC <sup>(1)</sup>		MAC <sup>(1)</sup> MPY <sup>(1)</sup> MPY.N <sup>(1)</sup> MSC <sup>(1)</sup>		MOVSAC <sup>(1)</sup>	SFTAC <sup>(1)</sup>	ADD <sup>(1)</sup>	LAC <sup>(1)</sup>	ADD <sup>(1)</sup> NEG <sup>(1)</sup> SUB <sup>(1)</sup>	SAC <sup>(1)</sup>				
	1101	SL	ASR LSR	RLC RLNC	RRC RRNC	SL	ASR LSR	RLC RLNC	RRC RRNC	DIV.S DIV.U	DIVF <sup>(1)</sup>	—	—	—				
	1110	CP0	CP CPB	CP0	СР СРВ		_	CPBGT <sup>(2)</sup> CPBLT <sup>(2)</sup> CPSGT CPSLT	CPBEQ <sup>(2)</sup> CPBNE <sup>(2)</sup> CPSEQ CPSNE	INC INC2	DEC DEC2	COM NEG	CLR SETM	INC INC2				
	1111		ED/ MA	)(1) <sub>\C</sub> (1) <sub>C</sub> (1) <sub>\Y</sub> (1)		—	_	_	_	PUSH	POP	LNK ULNK	SE ZE	DISI				

This instruction is only available in dsPIC30F, dsPIC33F, and dsPIC33E family devices. This instruction is only available in PIC24E and dsPIC33E family devices.

1: 2:

Note

Reference

7

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#### 7.2 INSTRUCTION SET SUMMARY TABLE

The complete 16-bit MCU and DSC device instruction set is summarized in Table 7-2. This table contains instruction set. It includes instruction assembly syntax, description, size (in 24-bit words), execution time ( Status bits, and the page number in which the detailed description can be found. Table 1-2 identifies the Instruction Set Summary Table.

The instruction cycle counts listed here are for PIC24F, PIC24H, dsPIC30F and dsPIC33F device Note: additional cycles in PIC24E and dsPIC33E devices. Refer to Section 3.3 "Instruction Set Su 5.4 "Instruction Descriptions" for details.

#### Table 7-2: Instruction Set Summary Table

	Assembly Syntax Mnemonic, Operands	Description	Words	Cycles	0A <sup>(2)</sup>	OB <sup>(2)</sup>	SA <sup>(1,2)</sup>	SB <sup>(1,2)</sup>	0AB <sup>(2)</sup>	SAB <sup>(1,2)</sup>	DC
ADD	f {,WREG}	Destination = f + WREG	1	1	_	_	—	—	-	-	¢
ADD	#lit10,Wn	Wn = lit10 + Wn	1	1	_	_	_	_	-	—	ţ
ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	_	_	—	—	—	_	¢
ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	_	_	—	—	_	_	ţ
ADD	Acc <sup>(2)</sup>	Add accumulators	1	1	Û	Û	Û	仓	ţ	仓	_
ADD	Wso,#Slit4,Acc	16-bit signed add to accumulator	1	1	Û	€	企	企	¢	仓	_
ADDC	f {,WREG}	Destination = f + WREG + (C)	1	1	—	—	—	_	—	_	ţ
ADDC	#lit10,Wn	Wn = lit10 + Wn + (C)	1	1	_	_	—	—	_	_	ţ
ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	—	_	_	_	_	_	ţ
ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	_	_	—	—	_	_	ţ
AND	f {,WREG}	Destination = f .AND. WREG	1	1	—	—	—	_	—	_	_
AND	#lit10,Wn	Wn = lit10 .AND. Wn	1	1	_	_	—	—	_	_	_
AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	_	_	—	—	_	_	_
AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	_	_	—	—	_	_	_
ASR	f {,WREG}	Destination = arithmetic right shift f, LSb $\rightarrow$ C	1	1	—	—	—	—	—	-	—
ASR	Ws,Wd	Wd = arithmetic right shift Ws, LSb $\rightarrow C$	1	1	—	_	—	—	-	-	—
ASR	Wb,#lit4,Wnd	Wnd = arithmetic right shift Wb by lit4, LSb $\rightarrow C$	1	1	—	_	_	_	_	_	—

Legend: 🕄 set or cleared; 🖟 may be cleared, but never set; 🕆 may be set, but never cleared; '1' always set; '0' always cleared; — unchanged Note

SA, SB and SAB are only modified if the corresponding saturation is enabled, otherwise unchanged. 1:

2: This instruction/operand is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.

This instruction/operand is only available in PIC24E and dsPIC33E devices. 3:

This instruction/operand is only available in dsPIC33E devices. 4:

5: This instruction/operand is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices.

	Assembly Syntax Mnemonic, Operands	Description	Words	Cycles	0A <sup>(2)</sup>	ов <sup>(2)</sup>	SA <sup>(1,2)</sup>	SB <sup>(1,2)</sup>	0AB <sup>(2)</sup>	SAB <sup>(1,2)</sup>	DC
ASR	Wb,Wns,Wnd	Wnd = arithmetic right shift Wb by Wns, LSb $\rightarrow$ C	1	1	_	_	_	_	_	_	_
BCLR	f,#bit4	Bit clear f	1	1	—	—	_	_	_	_	—
BCLR	Ws,#bit4	Bit clear Ws	1	1	_	_	—	—	—	_	—
BRA	Expr	Branch unconditionally	1	2	_	_	—	—	_	_	-
BRA	Wn	Computed branch	1	2	—	—	-	—	—	_	—
BRA	C,Expr	Branch if Carry	1	1 (2)		_	-	—	_	—	—
BRA	GE,Expr	Branch if greater than or equal	1	1 (2)	—	—	-	—	—	_	—
BRA	GEU,Expr	Branch if Carry	1	1 (2)	_	_	—	—	_	_	-
BRA	GT,Expr	Branch if greater than	1	1 (2)	—	—	-	—	—	_	—
BRA	GTU, Expr	Branch if unsigned greater than	1	1 (2)	—	_	-	_	_	_	—
BRA	LE,Expr	Branch if less than or equal	1	1 (2)		_	-	—	_	—	-
BRA	LEU, Expr	Branch if unsigned less than or equal	1	1 (2)	—	—	-	—	—	_	—
BRA	LT,Expr	Branch if less than	1	1 (2)	—	—	-	—	—	_	_
BRA	LTU, Expr	Branch if not Carry	1	1 (2)	—	—	-	—	—	_	—
BRA	N,Expr	Branch if Negative	1	1 (2)	—	—	-	—	—	_	_
BRA	NC,Expr	Branch if not Carry	1	1 (2)	—	_	-	_	_	_	_
BRA	NN,Expr	Branch if not Negative	1	1 (2)	_	_	—	—	—	_	—
BRA	NOV,Expr	Branch if not Overflow	1	1 (2)	_	_	—	—	—	_	—
BRA	NZ,Expr	Branch if not Zero	1	1 (2)	—	_	-	—	_	_	_
BRA	0A, Expr <sup>(2)</sup>	Branch if Accumulator A overflow	1	1 (2)	—	—	-	—	—	_	—
BRA	0B, Expr <sup>(2)</sup>	Branch if Accumulator B overflow	1	1 (2)	—	—	-	—	—	_	—
BRA	OV,Expr	Branch if Overflow	1	1 (2)	—	—	-	—	—	_	—
BRA	SA, Expr <sup>(2)</sup>	Branch if Accumulator A saturated	1	1 (2)	—	—	-	—	—	_	—
BRA	SB, Expr <sup>(2)</sup>	Branch if Accumulator B saturated	1	1 (2)	—	—	-	—	—	_	—
BRA	Z,Expr	Branch if Zero	1	1 (2)	_	_	—	—	—	_	—
BSET	f,#bit4	Bit set f	1	1	_	_	_	_	_	_	—
BSET	Ws,#bit4	Bit set Ws	1	1	—	—	-	—	—	—	—
BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	_	_	I —	—	—	—	

Note 1: SA, SB and SAB are only modified if the corresponding saturation is enabled, otherwise unchanged.

This instruction/operand is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices. 2:

This instruction/operand is only available in PIC24E and dsPIC33E devices. 3:

4: This instruction/operand is only available in dsPIC33E devices.

This instruction/operand is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices. 5:

6: This instruction/operand is only available in dsPIC30F and dsPIC33F devices.

Reference

	Assembly Syntax Mnemonic, Operands	Description	Words	Cycles	0A <sup>(2)</sup>	ОВ <sup>(2)</sup>	SA <sup>(1,2)</sup>	SB <sup>(1,2)</sup>	0AB <sup>(2)</sup>	SAB <sup>(1,2)</sup>	DC
BSW.Z	Ws,Wb	Write Z bit to Ws <wb></wb>	1	1	-	_		_	-	—	—
BTG	f,#bit4	Bit toggle f	1	1	_	_	_	_	_	—	_
BTG	Ws,#bit4	Bit toggle Ws	1	1	_	_	—	-	—	—	—
BTSC	f,#bit4	Bit test f, skip if clear	1	1 (2 or 3)			_	—	—	_	_
BTSC	Ws,#bit4	Bit test Ws, skip if clear	1	1 (2 or 3)		_	_	_	_	_	_
BTSS	f,#bit4	Bit test f, skip if set	1	1 (2 or 3)	_	_	_	_	_	_	_
BTSS	Ws,#bit4	Bit test Ws, skip if set	1	1 (2 or 3)			—	—	—	_	—
BTST	f,#bit4	Bit test f to Z	1	1		-	_	-	_		_
BTST.C	Ws,#bit4	Bit test Ws to C	1	1	_	_	_	-	-	—	—
BTST.Z	Ws,#bit4	Bit test Ws to Z	1	1	_	_	_	-	_	—	—
BTST.C	Ws,Wb	Bit test Ws <wb> to C</wb>	1	1	—	_	_	-	_	—	—
BTST.Z	Ws,Wb	Bit test Ws <wb> to Z</wb>	1	1		-	_	—	—	_	—
BTSTS	f,#bit4	Bit test f to Z, then set f	1	1	_	_	_	—	_	_	_
BTSTS.C	Ws,#bit4	Bit test Ws to C then set	1	1	_	_	_	_	_	_	—
BTSTS.Z	Ws,#bit4	Bit test Ws to Z then set	1	1	_	_	_	—	_	_	—
CALL	Expr	Call subroutine	2	2				—	_		—
CALL	Wn	Call indirect subroutine	1	2	-	_		—	—	_	—
CALL.L	Wn <sup>(3)</sup>	Call indirect subroutine (long address)	1	4			_	—	_	_	—
CLR	f	f = 0x0000	1	1			_	—	_	_	—
CLR	WREG	WREG = 0x0000	1	1				—		—	—
CLR	Wd	Wd = 0	1	1	_	—	_	—		_	—
CLR	Acc,[Wx],Wxd,[Wy],Wyd,AWB <sup>(2)</sup>	Clear accumulator	1	1	0	0	0	0	0	0	—
CLRWDT		Clear Watchdog Timer	1	1	_	_		_	_	_	_
СОМ	f {,WREG}	Destination = f	1	1		_	_	_	_	_	_
COM	Ws,Wd	$Wd = \overline{Ws}$	1	1		_	_	_	_		—

Table 7-2:	Instruction Set Summar	v Table (Continued)
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Legend: 🕄 set or cleared; 🖟 may be cleared, but never set; 🏦 may be set, but never cleared; '1' always set; '0' always cleared; 🛁 unchanged Note

SA, SB and SAB are only modified if the corresponding saturation is enabled, otherwise unchanged. 1:

2: This instruction/operand is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.

This instruction/operand is only available in PIC24E and dsPIC33E devices. 3:

4: This instruction/operand is only available in dsPIC33E devices.

5: This instruction/operand is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices.

	Assembly Syntax Mnemonic, Operands	Description	Words	Cycles	0A <sup>(2)</sup>	ОВ <sup>(2)</sup>	SA <sup>(1,2)</sup>	SB <sup>(1,2)</sup>	0AB <sup>(2)</sup>	SAB <sup>(1,2)</sup>	DC
СР	f	Compare (f – WREG)	1	1	_	_	—	_	_	_	ŷ
СР	Wb,#lit5	Compare (Wb – lit5)	1	1	_	_	_	—	_	-	Û
СР	Wb,#lit8	Compare (Wb – lit8)	1	1	_	_	_	—	_	-	Û
СР	Wb,Ws	Compare (Wb – Ws)	1	1		_	—	—	_	-	ŷ
CP0	f	Compare (f – 0x0000)	1	1	_	_	-	_	_	-	1
CP0	Ws	Compare (Ws – 0x0000)	1	1	—	-	—	—		—	1
СРВ	f	Compare with borrow (f – WREG – $\overline{C}$ )	1	1	_	_	-	_	_	-	ŷ
СРВ	Wb,#lit5	Compare with borrow (Wb – lit5 – $\overline{C}$ )	1	1	—	—	—	—	_	-	ţ
СРВ	Wb,#lit8	Compare with borrow (Wb – lit8 – $\overline{C}$ )	1	1	—		—	—		-	ţ
СРВ	Wb,Ws	Compare with borrow (Wb – Ws – $\overline{C}$ )	1	1	_	-	—	—	_	_	ŷ
CPBEQ	Wb,Wn,Expr <sup>(3)</sup>	Compare Wb with Wn, branch if =	1	1 (5)		_	-	_	_	_	—
CPBGT	Wb,Wn,Expr <sup>(3)</sup>	Signed Compare Wb with Wn, branch if >	1	1 (5)		_	-	_	_	—	—
CPBLT	Wb,Wn,Expr <sup>(3)</sup>	Signed Compare Wb with Wn, branch if <	1	1 (5)		_	_	_	_	—	—
CPBNE	Wb,Wn,Expr <sup>(3)</sup>	Compare Wb with Wn, branch if $\neq$	1	1 (5)		_	_	_	_	_	_
CPSEQ	Wb,Wn	Compare (Wb with Wn), skip if =	1	1 (2 or 3)	_	_	_	_	_	_	_
CPSGT	Wb,Wn	Signed Compare (Wb with Wn), skip if >	1	1 (2 or 3)	_	_	_	_	_	_	_
CPSLT	Wb,Wn	Signed Compare (Wb with Wn), skip if <	1	1 (2 or 3)	-		-	-	_	_	—
CPSNE	Wb,Wn	Compare (Wb with Wn), skip if ≠	1	1 (2 or 3)	-		-	-	_	_	—
DAW.B	Wn	Wn = decimal adjust Wn	1	1	—	—	—	—	_	-	—
DEC	f {,WREG}	Destination = $f - 1$	1	1	—	-	—	—		—	$\hat{v}$
DEC	Ws,Wd	Wd = Ws - 1	1	1	_	—	—	_	_	_	ঢ়
DEC2	f {,WREG}	Destination = $f - 2$	1	1	_	—	—	_	_	_	ঢ়
DEC2	Ws,Wd	Wd = Ws - 2	1	1	_	—	_	_	—	_	Û

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Legend: 🕄 set or cleared; 🖟 may be cleared, but never set; 🏦 may be set, but never cleared; '1' always set; '0' always cleared; 🛁 unchanged Note

SA, SB and SAB are only modified if the corresponding saturation is enabled, otherwise unchanged. 1:

This instruction/operand is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices. 2:

This instruction/operand is only available in PIC24E and dsPIC33E devices. This instruction/operand is only available in dsPIC33E devices. 3:

4:

5: This instruction/operand is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices.

Table 7-2:	Instruction	Set Summary	Table (	(Continued)	

	Assembly Syntax Mnemonic, Operands	Description	Words	Cycles	0A <sup>(2)</sup>	ОВ <sup>(2)</sup>	SA <sup>(1,2)</sup>	SB <sup>(1,2)</sup>	0AB <sup>(2)</sup>	SAB <sup>(1,2)</sup>	DC
DISI	#lit14	Disable interrupts for lit14 instruction cycles	1	1	_	_	-	_	_	_	_
DIV.S	Wm,Wn	Signed 16/16-bit integer divide, $Q \rightarrow Wo, R \rightarrow W1$	1	18		-	—	—	—	_	—
DIV.SD	Wm,Wn	Signed 32/16-bit integer divide, $Q \rightarrow Wo, R \rightarrow W1$	1	18	_	_	—	_	—	_	_
DIV.U	Wm,Wn	Unsigned 16/16-bit integer divide, Q $\rightarrow$ Wo, R $\rightarrow$ W1	1	18	_	_	—	—	—	—	_
DIV.UD	Wm,Wn	Unsigned 32/16-bit integer divide, $Q \rightarrow Wo, R \rightarrow W1$	1	18	_	_	_	_	_	_	_
DIVF	Wm, Wn <sup>(2)</sup>	Signed 16/16-bit fractional divide, Q $\rightarrow$ Wo, R $\rightarrow$ W1	1	18	_	_	_	_	_	_	_
DO	#lit14,Expr <sup>(6)</sup>	Do code to PC + Expr, (lit14 + 1) times	2	2	_	_	_	_	_	_	_
DO	#lit15,Expr <sup>(4)</sup>	Do code to PC + Expr, (lit15 + 1) times	2	2	-	_	_	_	_	_	_
DO	Wn,Expr <sup>(2)</sup>	Do code to PC + Expr, (Wn + 1) times	2	2	—	—	_	_	_	—	—
ED	Wm*Wm,Acc,[Wx],[Wy],Wxd <sup>(2)</sup>	Euclidean distance (no accumulate)	1	1	$\hat{v}$	ţ	仓	仓	ţ	Û	-
EDAC	Wm*Wm,Acc,[Wx],[Wy],Wxd <sup>(2)</sup>	Euclidean distance	1	1	€	Û	仓	仓	Û	Û	_
EXCH	Wns,Wnd	Swap Wns and Wnd	1	1			—	—	_	_	—
FBCL	Ws,Wnd	Find bit change from left (MSb) side	1	1	—	_	_	_	_	_	_
FF1L	Ws,Wnd	Find first one from left (MSb) side	1	1	—	_	_	_	_	_	_
FF1R	Ws,Wnd	Find first one from right (LSb) side	1	1		_	—	—	_		_
GOTO	Expr	Go to address	2	2	_	_	_	_	_	_	_
GOT0	Wn	Go to address indirectly	1	2		-	—	—	—	_	—
GOTO.L	Wn <sup>(3)</sup>	Go to address indirectly (long address)	1	4			-		-	—	_
INC	f {,WREG}	Destination = f + 1	1	1			_	_	_	—	Û
INC	Ws,Wd	Wd = Ws + 1	1	1	—	—	-		-	—	Û
INC2	f {,WREG}	Destination = f + 2	1	1	—	_	_	_	_	_	Û
INC2	Ws,Wd	Wd = Ws + 2	1	1		-	—	—	—	_	Û
IOR	f {,WREG}	Destination = f .IOR. WREG	1	1	—	_	_	_	_	_	_
IOR	#lit10,Wn	Wn = lit10 .IOR. Wn	1	1	_	_	—	_	—	_	_
IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	_	—	—	_	—	—	_
IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	—	—	—	_	—	_	_
LAC	Wso,#Slit4, Acc <sup>(2)</sup>	Load accumulator	1	1	ţ	Û	仓	仓	Û	Û	—

🕄 set or cleared; 🖟 may be cleared, but never set; 🏦 may be set, but never cleared; '1' always set; '0' always cleared; 🛁 unchanged Legend: Note

SA, SB and SAB are only modified if the corresponding saturation is enabled, otherwise unchanged. This instruction/operand is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices. 1:

2:

3: This instruction/operand is only available in PIC24E and dsPIC33E devices.

4:

This instruction/operand is only available in dsPIC33E devices. This instruction/operand is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices. 5:

	Assembly Syntax Mnemonic, Operands	Description	Words	Cycles	0A <sup>(2)</sup>	ОВ <sup>(2)</sup>	SA <sup>(1,2)</sup>	SB <sup>(1,2)</sup>	0AB <sup>(2)</sup>	SAB <sup>(1,2)</sup>	DC
LNK	#lit14	Link Frame Pointer	1	1	—	_	_	_		_	—
LSR	f {,WREG}	Destination = logical right shift f, MSb $\rightarrow$ C	1	1	_	_	_	_	_		—
LSR	Ws,Wd	Wd = logical right shift Ws, MSb $\rightarrow$ C	1	1	_	_	_	_	_	_	<u> </u>
LSR	Wb,#lit4,Wnd	Wnd = logical right shift Wb by lit4, MSb $\rightarrow$ C	1	1	_	_	_	_		_	—
LSR	Wb,Wns,Wnd	Wnd = logical right shift Wb by Wns, MSb $\rightarrow$ C	1	1	_	_	_	_		_	—
MAC	Wm*Wn,Acc,[Wx],Wxd,[Wy], Wyd,AWB <sup>(2)</sup>	Multiply and accumulate	1	1	€	ţ	仓	仓	Û	仓	-
MAC	Wm*Wm,Acc,[Wx],Wxd,[Wy], Wyd <sup>(2)</sup>	Square and accumulate	1	1	ţ	¢	仓	仓	ţ	Û	-
MOV	f {,WREG}	Move f to destination	1	1	_	_	—	—			—
MOV	WREG, f	Move WREG to f	1	1	_	_	_	_	_	—	
MOV	f,Wnd	Move f to Wnd	1	1	_	_	—	—	_		—
MOV	Wns,f	Move Wns to f	1	1	_	_	—	—	_	_	—
MOV.B	#lit8,Wnd	Move 8-bit unsigned literal to Wnd	1	1	_	_	—	—	_	_	—
MOV	#lit16,Wnd	Move 16-bit literal to Wnd	1	1	_	_	—	—	_	_	—
MOV	[Ws+Slit10],Wnd	Move [Ws + Slit10] to Wnd	1	1	_	_	_	_	_	—	—
MOV	Wns,[Wd+Slit10]	Move Wns to [Wd + Slit10]	1	1	_	_	_	_	_	—	—
MOV	Wso,Wdo	Move Wso to Wdo	1	1		_	_	_		_	—
MOV.D	Wns,Wnd	Move double Wns to Wnd:Wnd + 1	1	2	_	_	—	—	_		—
MOV.D	Wns,Wnd	Move double Wns:Wns + 1 to Wnd	1	2		_	_	_	_		—
MOVPAG	#lit10,DSRPAG <sup>(3)</sup>	Move 10-bit literal to DSRPAG	1	1	_	_	—	—	_		—
MOVPAG	#lit9,DSWPAG <sup>(3)</sup>	Move 9-bit literal to DSWPAG	1	1	_	_	—	—	_		_
MOVPAG	#lit8,TBLPAG <sup>(3)</sup>	Move 8-bit literal to TBLPAG	1	1	_	_	—	—	_		—
MOVPAG	Wn, DSRPAG <sup>(3)</sup>	Move Wn to DSRPAG	1	1	_	_	_	_	_	—	—
MOVPAG	Wn,DSWPAG <sup>(3)</sup>	Move Wn to DSWPAG	1	1	_	_	_	_	_	_	_
MOVPAG	Wn, TBLPAG <sup>(3)</sup>	Move Wn to TBLPAG	1	1	—	_	—	_		—	—
MOVSAC	Acc,[Wx],Wxd,[Wy],Wyd,AWB <sup>(2)</sup>	Move [Wx] to Wxd, and [Wy] to Wyd	1	1	—	_	—	_	—	—	—
MPY	Wm*Wn,Acc,[Wx],Wxd,[Wy], Wyd <sup>(2)</sup>	Multiply Wn by Wm to accumulator	1	1	ţ	ţ	Û	Û	ţ	Û	

Legend: 🗘 set or cleared; 🖟 may be cleared, but never set; 🏦 may be set, but never cleared; '1' always set; '0' always cleared; — unchanged

SA, SB and SAB are only modified if the corresponding saturation is enabled, otherwise unchanged. This instruction/operand is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices. Note 1:

2:

3: This instruction/operand is only available in PIC24E and dsPIC33E devices.

4: This instruction/operand is only available in dsPIC33E devices.

This instruction/operand is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices. 5:

Table 7-2:	Instruction Set Summar	y Table	(Continued)	)
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	Assembly Syntax Mnemonic, Operands	Description	Words	Cycles	0A <sup>(2)</sup>	0B <sup>(2)</sup>	SA <sup>(1,2)</sup>	SB <sup>(1,2)</sup>	0AB <sup>(2)</sup>	SAB <sup>(1,2)</sup>	DC
MPY	Wm*Wm,Acc,[Wx],Wxd,[Wy], Wyd <sup>(2)</sup>	Square to accumulator	1	1	€	Ŷ	Û	Û	¢	Û	-
MPY.N	Wm*Wn,Acc,[Wx],Wxd,[Wy], Wyd <sup>(2)</sup>	-(Multiply Wn by Wm) to accumulator	1	1	0	0	_	_	0	_	-
MSC	Wm*Wn,Acc,[Wx],Wxd,[Wy], Wyd,AWB <sup>(2)</sup>	Multiply and subtract from accumulator	1	1	⇔	Û	Û	Û	ŷ	仓	-
MUL	f	W3:W2 = f * WREG	1	1	—	_	_	_	-	_	—
MUL.SS	Wb,Ws,Wnd	{Wnd + 1,Wnd} = signed(Wb) * signed(Ws)	1	1	—	_	_	_	-	_	—
MUL.SS	Wb,Ws,Acc <sup>(4)</sup>	Accumulator = signed(Wb) * signed(Ws)	1	1	_	—	_	_	-	—	—
MUL.SU	Wb,#lit5,Wnd	{Wnd + 1,Wnd} = signed(Wb) * unsigned(lit5)	1	1	_	—	_	_	-	—	—
MUL.SU	Wb,Ws,Wnd	{Wnd + 1,Wnd} = signed(Wb) * unsigned(Ws)	1	1	—	_	_		-	—	—
MUL.SU	Wb,Ws,Acc <sup>(4)</sup>	Accumulator = signed(Wb) * unsigned(Ws)	1	1	—	_	_		-	—	—
MUL.SU	Wb,#lit5,Acc <sup>(4)</sup>	Accumulator = signed(Wb) * unsigned(lit5)	1	1	—	_	_		-	—	—
MUL.US	Wb,Ws,Wnd	{Wnd + 1,Wnd} = unsigned(Wb) * signed(Ws)	1	1	—		_	—	—	_	—
MUL.US	Wb,Ws,Acc <sup>(4)</sup>	Accumulator = unsigned(Wb) * signed(Ws)	1	1	—	_	_	_	-	_	—
MUL.UU	Wb,#lit5,Wnd	{Wnd + 1,Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	-	_	-		-	_	—
MUL.UU	Wb,Ws,Wnd	{Wnd + 1,Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	_	_	_	_	-	_	—
MUL.UU	Wb,Ws,Acc <sup>(4)</sup>	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	—	_	_		-	—	—
MUL.UU	Wb,#lit5,Acc <sup>(4)</sup>	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	—	_	_		-	—	—
MULW.SS	6 Wb,Ws,Wnd <sup>(3)</sup>	Wnd = signed(Wb) * signed(Ws)	1	1	—	_	_		-	—	—
MULW.SU	J Wb,Ws,Wnd <sup>(3)</sup>	Wnd = signed(Wb) * unsigned(Ws)	1	1	—	_	_		-	—	—
MULW.SU	J Wb,#lit5,Wnd <sup>(3)</sup>	Wnd = signed(Wb) * unsigned(lit5)	1	1	-	_			-	—	—
MULW.US	8 Wb,Ws,Wnd <sup>(3)</sup>	Wnd = unsigned(Wb) * signed(Ws)	1	1	-	_			-	—	—
MULW.UU	J Wb,Ws,Wnd <sup>(3)</sup>	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	_	—	_	_	-	—	—
MULW.UU	J Wb,#lit5,Wnd <sup>(3)</sup>	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	-	—	-		-	—	—
NEG	f {,WREG}	Destination = $\overline{f}$ + 1	1	1	_	_			_	_	ŷ
NEG	Ws,Wd	$Wd = \overline{Ws} + 1$	1	1	_	_	—		—	_	Û
NEG	Acc <sup>(2)</sup>	Negate accumulator	1	1	¢	Û	仓	仓	Û	仓	—
NOP		No operation	1	1	_				_	_	_

 $\hat{1}$  set or cleared;  $\hat{-}$  may be cleared, but never set;  $\hat{1}$  may be set, but never cleared; '1' always set; '0' always cleared; - unchanged SA, SB and SAB are only modified if the corresponding saturation is enabled, otherwise unchanged. Legend: Note

1:

2: This instruction/operand is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.

This instruction/operand is only available in PIC24E and dsPIC33E devices. 3:

This instruction/operand is only available in dsPIC33E devices. 4:

This instruction/operand is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices. 5:

	Assembly Syntax Mnemonic, Operands	Description	Words	Cycles	0A <sup>(2)</sup>	ов <sup>(2)</sup>	SA <sup>(1,2)</sup>	SB <sup>(1,2)</sup>	0AB <sup>(2)</sup>	SAB <sup>(1,2)</sup>	DC
NOPR		No operation	1	1	—	_	—	—		_	—
POP	f	POP TOS to f	1	1	_	_	_	_	_	—	—
POP	Wdo	POP TOS to Wdo	1	1	_	_	—	_	_	—	—
POP.D	Wnd	POP double from TOS to Wnd:Wnd + 1	1	2	_	—	-	—	—	_	—
POP.S		POP shadow registers	1	1	_	_	_	_	_		Û
PUSH	f	PUSH f to TOS	1	1	_	—	-	—	—	_	—
PUSH	WSO	PUSH Wso to TOS	1	1	_	—	-	—	—	_	—
PUSH.D	Wns	PUSH double Wns:Wns + 1 to TOS	1	2		_	—	—			—
PUSH.S		PUSH shadow registers	1	1		_	—	—			—
PWRSAV	#lit1	Enter Power-saving mode	1	1	_	_	-	_	_	—	—
RCALL	Expr	Relative call	1	2	—	_	—	_	_	—	—
RCALL	Wn	Computed call	1	2	—	_	—		_	_	—
REPEAT	#lit14 <sup>(5)</sup>	Repeat next instruction (lit14 + 1) times	1	1	—	_	-		_	_	—
REPEAT	#lit15 <sup>(3)</sup>	Repeat next instruction (lit15 + 1) times	1	1	—	_	-		_	_	—
REPEAT	Wn	Repeat next instruction (Wn + 1) times	1	1			_		_	—	—
RESET		Software device Reset	1	1		_	—	_		_	—
RETFIE		Return from interrupt enable	1	3 (2)	-	_	_	_	_	_	—
RETLW	#lit10,Wn	Return with lit10 in Wn	1	3 (2)	—	_	-	_	_	—	—
RETURN		Return from subroutine	1	3 (2)	—	_	-		_	_	—
RLC	f {,WREG}	Destination = rotate left through Carry f	1	1	—		—			—	—
RLC	Ws,Wd	Wd = rotate left through Carry Ws	1	1		_	_	_	_	_	_
RLNC	f {,WREG}	Destination = rotate left (no Carry) f	1	1	_	_	_	_	_		—
RLNC	Ws,Wd	Wd = rotate left (no Carry) Ws	1	1	—	_	_	_	_	_	—
RRC	f {,WREG}	Destination = rotate right through Carry f	1	1	_	—	-	—	—	—	—
RRC	Ws,Wd	Wd = rotate right through Carry Ws	1	1	_	—	-	—	—	—	—
RRNC	f {,WREG}	Destination = rotate right (no Carry) f	1	1			—	_	_	—	
RRNC	Ws,Wd	Wd = rotate right (no Carry) Ws	1	1	-		_	—		—	—
SAC	Acc,#Slit4,Wdo <sup>(2)</sup>	Store accumulator	1	1	—	—	-	—	—	—	—

Legend: 🕄 set or cleared; 🖟 may be cleared, but never set; 🕆 may be set, but never cleared; '1' always set; '0' always cleared; — unchanged Note

SA, SB and SAB are only modified if the corresponding saturation is enabled, otherwise unchanged. 1:

This instruction/operand is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices. 2:

3: This instruction/operand is only available in PIC24E and dsPIC33E devices.

This instruction/operand is only available in dsPIC33E devices. 4:

This instruction/operand is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices. 5:

6: This instruction/operand is only available in dsPIC30F and dsPIC33F devices.

Reference

	Assembly Syntax Mnemonic, Operands	Description	Words	Cycles	0A <sup>(2)</sup>	ОВ <sup>(2)</sup>	SA <sup>(1,2)</sup>	SB <sup>(1,2)</sup>	0AB <sup>(2)</sup>	SAB <sup>(1,2)</sup>	DC
SAC.R	Acc,#Slit4,Wdo <sup>(2)</sup>	Store rounded Accumulator	1	1	-	_	-	—	_	—	_
SE	Ws,Wd	Wd = sign-extended Ws	1	1	—	—	—	—	—	—	—
SETM	f	f = 0xFFFF	1	1	—	—	—	—	—	—	—
SETM	WREG	WREG = 0xFFFF	1	1		_	-	—	_	—	-
SETM	Wd	Wd = 0xFFFF	1	1	—	—	—	—	—	—	—
SFTAC	Acc,#Slit6 <sup>(2)</sup>	Arithmetic shift accumulator by Slit6	1	1	€	€	企	Û	$\hat{\mathbf{v}}$	仓	-
SFTAC	Acc,Wb <sup>(2)</sup>	Arithmetic shift accumulator by (Wb)	1	1	ţ	Û	仓	仓	Û	仓	-
SL	f {,WREG}	Destination = arithmetic left shift f	1	1	_	_	_	-	_	—	_
SL	Ws,Wd	Wd = arithmetic left shift Ws	1	1	_	_	_	-	_	—	—
SL	Wb,#lit4,Wnd	Wnd = left shift Wb by lit4	1	1	—	—	—	—	—	—	_
SL	Wb,Wns,Wnd	Wnd = left shift Wb by Wns	1	1	_	_	_	—	_	—	_
SUB	f {,WREG}	Destination = f – WREG	1	1	_	_	_	_	_	_	ţ
SUB	#lit10,Wn	Wn = Wn - lit10	1	1	—	—	_	_	_	_	ţ
SUB	Wb,#lit5,Wd	Wd = Wb - lit5	1	1	_	_	_	_	_	_	ţ
SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	_	_	_	_	_	—	ţ
SUB	Acc <sup>(2)</sup>	Subtract accumulators	1	1	Û	Û	仓	仓	Û	仓	_
SUBB	f {,WREG}	destination = f – WREG – $(\overline{C})$	1	1	_	_	_	_	_	—	ţ
SUBB	#lit10,Wn	Wn = Wn – lit $10 - (\overline{C})$	1	1	_	_	_	—	_	_	€
SUBB	Wb,#lit5,Wd	$Wd = Wb - lit5 - (\overline{C})$	1	1	—	—	—	—	—	—	€
SUBB	Wb,Ws,Wd	$Wd = Wb - Ws - (\overline{C})$	1	1	—	—	—	—	_	_	ţ
SUBBR	f {,WREG}	Destination = WREG – f – $(\overline{C})$	1	1	_	_	_	—	_	—	ţ
SUBBR	Wb,#lit5,Wd	$Wd = lit5 - Wb - (\overline{C})$	1	1	_	_	_	_	_	_	ţ
SUBBR	Wb,Ws,Wd	$Wd = Ws - Wb - (\overline{C})$	1	1	—	—	_	—	_	_	ţ
SUBR	f {,WREG}	Destination = WREG – f	1	1	_	_	_	—	_	—	ţ
SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	_	—	_	—	_	_	ţ
SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	—	—	—	—	—	—	ţ
SWAP	Wn	Wn = byte or nibble swap Wn	1	1	_	_	_	<u> </u>	_	_	_

Legend:  $\hat{v}$  set or cleared;  $\Psi$  may be cleared, but never set;  $\hat{v}$  may be set, but never cleared; '1' always set; '0' always cleared; — unchanged Note

SA, SB and SAB are only modified if the corresponding saturation is enabled, otherwise unchanged. 1:

This instruction/operand is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices. This instruction/operand is only available in PIC24E and dsPIC33E devices. 2:

3:

4: This instruction/operand is only available in dsPIC33E devices.

5: This instruction/operand is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices.

	Assembly Syntax Mnemonic, Operands	Description	Words	Cycles	0A <sup>(2)</sup>	ОВ <sup>(2)</sup>	SA <sup>(1,2)</sup>	SB <sup>(1,2)</sup>	0AB <sup>(2)</sup>	SAB <sup>(1,2)</sup>	DC
TBLRDH	[Ws],Wd	Read high program word to Wd	1	2	—	_	—	_	_	—	—
TBLRDL	[Ws],Wd	Read low program word to Wd	1	2	_	_	-	_	—	—	—
TBLWTH	Ws,[Wd]	Write Ws to high program word	1	2	_	_	-	_	—	—	—
TBLWTL	Ws,[Wd]	Write Ws to low program word	1	2	_	_	-	_	—	—	—
ULNK		Unlink Frame Pointer	1	1	_	_	_	_	_	—	—
XOR	f {,WREG}	Destination = f .XOR. WREG	1	1	—	_	_	_	_	—	—
XOR	#lit10,Wn	Wn = lit10 .XOR. Wn	1	1	-	_	_	_	—	_	—
XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	_	_	_		—	—	_
XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	—	_	_	_	_	-	_
ZE	Ws,Wnd	Wnd = zero-extended Ws	1	1	_	_	_	_	_	—	_

Legend: 🕄 set or cleared; 🔱 may be cleared, but never set; 🕆 may be set, but never cleared; '1' always set; '0' always cleared; 🛁 unchanged Note

1: SA, SB and SAB are only modified if the corresponding saturation is enabled, otherwise unchanged.

2: This instruction/operand is only available in dsPIC30F, dsPIC33F, and dsPIC33E devices.

3: This instruction/operand is only available in PIC24E and dsPIC33E devices.

4: This instruction/operand is only available in dsPIC33E devices.

This instruction/operand is only available in PIC24F, PIC24H, dsPIC30F, and dsPIC33F devices. 5:

## 7.3 REVISION HISTORY

## Revision A (May 2005)

This is the initial release of this document.

## **Revision B (September 2005)**

This revision incorporates all known errata at the time of this document update.

## **Revision C (February 2008)**

This revision includes the following corrections and updates:

- Instruction Updates:
  - Updated BRA Instruction (see "BRA")
  - Updated DIVF Instruction (see "DIVF")
  - Updated D0 Instruction (see "DO")
  - Updated SUB instruction (see "SUB")

## **Revision D (November 2009)**

This revision includes the following corrections and updates:

- Document renamed from dsPIC30F/33F Programmer's Reference Manual to 16-bit MCU and DSC Programmer's Reference Manual
- Document has been completely redesigned to accommodate all current 16-bit families: dsPIC30F, dsPIC33F, PIC24F and PIC24H

## Revision E (June 2010)

This revision includes the following corrections and updates:

 Information specific to dsPIC33E and PIC24E devices has been added throughout the document

## Revision F (July 2011)

This revision includes the following corrections and updates:

- Added a new section "Built-in Functions"
- Added and updated the cross-references throughout the document
- Updated the bit characteristics from U to U-0 in Register 2-4 and Register 2-6
- Added a note throughout the document specifying the requirement of an additional cycle for read and read-modify-write operations on non-CPU special function registers in dsPIC33E and PIC24E devices
- · Updates to formatting and minor text changes were incorporated throughout the document

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